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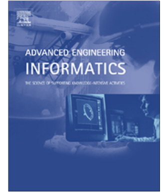

Full length article

Hypergraphs and extremal optimization in 3D integrated circuit design automation

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A B S T R A C T

The circuit design task poses an extremely difficult intellectual challenge. The solution has to meet a number of specific requirements and satisfy a variety of constraints. Efficient search of huge and discontinuous spaces requires new non-deterministic and heuristic algorithms. The goal of the research is to minimize the total wire-length of interconnects between sub-circuits. The paper presents a knowledge intensive 3D ICs layout hypergraph representation together with the elaborated neighborhood optimization heuristics. The results of the Extremal Optimization (EO) implementation applied to the MCNC set of benchmark circuits are reported.

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1. Introduction

The spatial arrangement of components which complies with the given requirements and satisfies the set of various constraints is one of the fundamental engineering design tasks. Among the others, it applies to floorplanning of integrated circuits (IC) design, building model generation or building reconstruction. It is important not only for scientific research and everyday practical problems, such as urban planning, crisis management or analysis of alternative energy sources, but also for entertainment or virtual reality modeling. It may take several years of work by a team of specialists to generate an artificial complex and developed 3D environment. Thus, efficient search of manifold spaces requires new non-deterministic and heuristic solutions. Especially architectural design [28] and integrated circuits floorplanning [29] are the fields where the automatic generation of three-dimensional (3D) spatial configurations is a priority task.

Most advanced integration technologies based on silicon are fast approaching their physical limits. Device (transistor) scaling is reaching the atomic distances. When we are talking about 14 nm or maybe 10 nm technologies one has to bear in mind that the distance between atoms in the silicon crystal are 3.12 nm! How much further can we go? Also for these extremely small devices so-called short channel effects play predominant role causing malfunctioning of the devices.

Another very serious problem are interconnects – how effectively connect billions of devices on a chip? In the planar technologies about 80% of the area of the chip is used by interconnect wires. Long interconnects have several adverse effects on the efficiency of operation of the circuits. The ratio between signal delay and the operation delay in the processor chips reaches the factor of 10 or more. Power dissipation along the interconnect lines becomes a problem by itself. On a planar structure most of the interconnects are built using successive metal layers superimposed over the silicon and isolated by oxidation between each-other. In the search for better efficiency, using smaller material (silicon) footprint, reducing power dissipation, small time delays researchers came with the idea of putting the building blocks or sub-circuits into a three-dimensional structure. This offers very significant reduction in connection length and signal delays. Short vertical interconnect can replace long in-plane wires when blocks are positioned in a right way. This advantage comes however on the expense of many technological problems and very high cost. Most certainly 3D integration will be the technology which will come more and more into new commercial application. This in turn implies that new placement and routing methodologies dedicated for 3D geometries have to be developed.

One of the key stages in electronic design is floorplanning ie. positioning of the components, sub-circuits and building blocks within the given area/volume. A floorplan has to be designed in accordance with the given set of requirements and comply with the preset restrictions. While searching for the right floorplan solution, some architectural decisions are evaluated and chip area together with delay and congestion caused by wiring are estimated. Even though the task has been effectively solved in two-dimensional (2D) spaces, the third dimension cannot be easily adopted to the elaborated algorithmic approaches. The computational complexity and the solution space of the task in 3D is much

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greater than the one in 2D [24] and stochastic methods are needed to obtain a globally near-optimal solution.

In [14] a novel approach to 3D ICs layout design has been presented. The proposed method is generic and separates the optimization methodology from the semantic layer of the specific design task, and from the presentation layer, which is responsible for displaying the flow of search space exploration. The design knowledge is provided in the form of predicates that are fed into the generation and optimization procedures. The designer defines a simple shape grammar. The shape grammar supervised by the intelligent derivation controller generates feasible candidate design solutions. The overall search time may be drastically reduced by application of the emergence phenomenon. Recognizable emergent structures, like gaps (empty spaces), that are not represented in the design explicitly but emerge from it, can be localized and incorporated into the generation procedure. The total wire-length of the achieved result may be further optimized with the use of a knowledge intensive 3D ICs layout hypergraph representation [15] together with the elaborated neighborhood optimization heuristics [16]. This paper gathers and develops the results of our previous work published in [14,15,17]. The current goal of the research is to minimize the total wire-length of interconnects between sub-circuits. The results of the Extremal Optimization (EO) implementation applied to the Microelectronics Center of North Carolina (MCNC) set of benchmark circuits are reported [26].

The paper is organized as follows. Section 2 presents most popular floorplan representations, namely sequence pair, bounded slice-line grid, O-tree, B*-tree, corner block list, and transitive closure graph. It also introduces proposed hierarchical layout hypergraph representation. Section 3 describes elaborated hypergraph topological partitioning approach together with its extremal optimization implementation. In the next section (Section 4) the experimental results of the proposed method applied to the MCNC set of benchmark circuits are reported. The last section of the paper contains conclusions.

2. Floorplan representation

The aim of integrated circuits physical design is to elaborate a geometrically and functionally correct representation of an IC. Given components' electrical and physical properties from technology library information and the connection topology from the netlist, the goal is to determine the spatial arrangement of components and their connections within the IC layout. A netlist is the collection of all signal nets and the components that they connect in a design, in other words, a list of all the nets and connecting pins. The entire geometrical arrangement of components is called a floorplan [21].

There are different, sometimes conflicting, floorplanning optimization goals, just to mention the bounding box minimization, the total wire-length minimization, the signal delays optimization, or the hot spot problem reduction. Since the task is to pack all the components in a chip without violating design rules, it is a kind of the box packing problem where many functional and production requirements must be met. The minimum bounding box of such a packing is called the chip [29] and it requires packing individual components densely together. The analogous situation is recorded in case of the wire-length reduction where shortening connections enlarges packaging density. Long connections may increase signal propagation delays and manufacturing cost. On the other hand, when the packing is overly dense in a particular region, the hot spot problem may occur. Thermal management requires settling the most heating components in the chip peripheries and sometimes spreading them further apart which may increment chip size, wire length and manufacturing cost.

There are many commercial electronic design automation (EDA) tools for 2D ICs layout design. Floorplans may be classified into two categories: slicing floorplans [33,31], and the non-slicing ones. A slicing floorplan is obtained by recursively cutting the floorplan horizontally or vertically [29]. In this case, the solution space is restricted which implies a simpler data structures representation and a faster runtime. However, a non-slicing structure is more general and suitable for most of the real design examples. Hence, various non-slicing floorplan representations have been proposed, namely sequence pair (SP) [27], bounded slice-line grid (BSG) [30], O-tree [18], B*-tree [5], corner block list (CBL) [20], and transitive closure graph (TCG) [25].

A *sequence pair* (SP) [27] is an ordered pair of component name permutations (Γ_+, Γ_-). The two permutations together represent geometric relations between every pair of components x and y by one of four ways: x is right of y, x is below y, x is above y, x is left of y. Specifically, if x appears before y in both Γ_+ and Γ_-, then x is to the left of y. If x appears before y in Γ_+ and after y in Γ_-, then x is above y. If x appears after y in Γ_+ and before y in Γ_-, then x is below y. Otherwise, if x appears after y in both Γ_+ and Γ_-, then x is to the right of y. The constraint imposed on the packing by a sequence pair is unique. Two directed *constraint graphs* constitute an intermediate representation between SP and floorplans. Even though constraint graphs are not compute by modern SP algorithms they are very useful for a better conceptual understanding. A vertical constraint graph captures *below-above* relations between components while a horizontal constraint graph depicts *to the left-to the right* ones. Fig. 1 illustrates a sample floorplan and its corresponding sequence pair and constraint graphs.

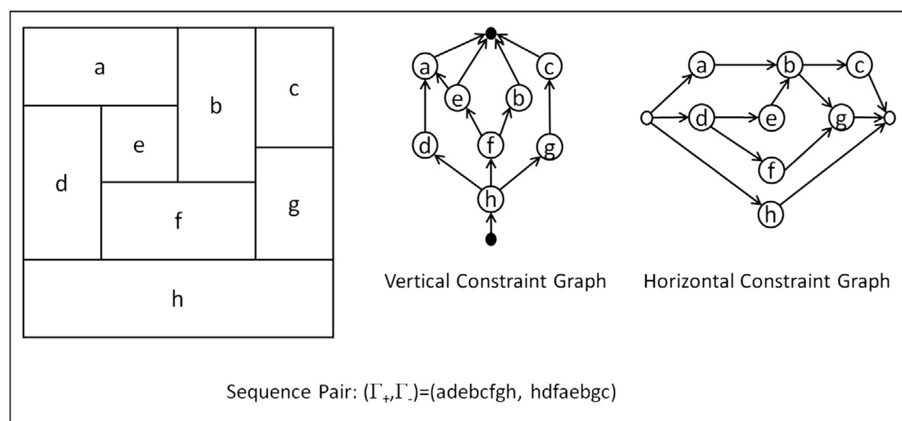

Fig. 1. Example floorplan of components a–h, its vertical constraint graph, its horizontal constraint graph, and its sequence pair.

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