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Control of device characteristics by passivation of graphene field effect transistors with polymers



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ABSTRACT

We investigate the possibility of controlling electrical characteristics of graphene-based field effect transistors (GRFETs) by passivating top or bottom surface of graphene with polymers. As-fabricated GRFETs made of graphene synthesized with chemical vapor deposition and transferred to a Si/SiO₂ substrate typically exhibit p-type doping and hysteresis originated from polymer residue and O₂/H₂O in the ambient atmosphere. We applied poly(vinyl alcohol, PVA) and polydimethylsiloxane (PDMS) and their stacks as passivation layers on graphene at the bottom or top surface to control device characteristics. Depending on the polymer, n-type doping (compensation of p-type doping), suppression of hysteresis, and enhancement of mobility are observed. Air stability of the passivation methods is also investigated.

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1. Introduction

Since the first demonstration of atomically thin layers of graphite on the surface [1], graphene, a two-dimensional (2D) material consisting of sp^2 bonded carbon atoms [2,3], has been under active investigations and researches to date [4,5]. Graphene has shown potentials in diverse applications such as electronic [6,7] or photonic devices [8,9], energy materials/devices [10], and composite materials [11]. As an electronic material, graphene has zero bandgap [12], which makes its application as a logic device difficult or ineffective. However, due to its high mobility and intrinsic flexibility, graphene still shows its promise as electronic device for such applications as high-speed [13] and flexible electronic devices [14]. For such applications, graphene synthesized by chemical vapor deposition (CVD) is often used for scale-up production and device fabrications [15,16]. Graphene field effect transistors (GRFETs) made of either exfoliated or transferred CVD-grown graphene often exhibit p-type doping and hysteresis in the ambient condition [17–23]. P-type doping in graphene is usually attributed to fixed charges in polymer residue (such as PMMA which is used for the transfer of graphene from Cu substrate or photoresist) and a

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the interface between bottom of the graphene and the substrate [23]. Since these effects are usually detrimental for device applications, identifying the origin of these effects and their control are essential. Various approaches have been tried for controllable doping of graphene. Substitutional doping similar to bulk semiconductor as well as surface transfer doping has been tried with some successes [24–32]. Hysteresis is usually unavoidable in ambient condition due to the presence of water. Therefore, passivation with hydrophobic material is often used to suppress the hysteresis [18,30]. Since 2D materials such as graphene is well suited for future flexible devices, any passivation or doping method needs to be compatible with flexibility of the host material. In this aspect, some polymers have been explored for possible doping and passivation of graphene [26,28,29]. In this contribution, we report passivation of GRFETs using poly(vinyl alcohol, PVA), polydimethylsiloxane (PDMS), and their

redox reaction involving H_2O/O_2 [19,22]. On the other hand, hysteresis is related to H_2O adsorption on top of graphene as well as at

poly(vinyl alcohol, PVA), polydimethylsiloxane (PDMS), and their stacks. We investigated passivation effects of polymers by comparing device characteristics of the same devices before and after passivation of either bottom or top surface of graphene. We found that doping in graphene can be controlled with the top passivation by PVA while passivation with PDMS can stabilize the doping effect by reducing water adsorption.







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2. Material and methods

Graphene is grown by low pressure CVD using a Cu foil (25 mm thick, from Alfa Aesar) as a catalytic growth substrate and CH₄ as a carbon feedstock gas at the growth temperature of 1000 °C [16]. Before the growth, the Cu foil is first etched in ammonium peroxydisulfate [(NH₄)₂S₂O₈] solution for 1 min to remove the surface copper oxide. Then, the Cu foil is annealed in H₂ atmosphere at the growth temperature for 1 h before graphene is grown with the mixture of CH₄ and H₂ gas. After 1 h growth, fully covered single layer graphene is obtained. After the growth, wet transfer method with PMMA is used to prepare graphene on Si/SiO₂ surface for device fabrications [33]. After the transfer to a Si substrate (with 200 nm-thick SiO₂), electrode patterns are defined by photolithography and electrodes are formed by e-beam evaporation of 1.5 nm-thick Ti (adhesion layer) and 30 nm-thick Au, and a lift-off process. Graphene channels with various widths are prepared with another round of photolithography to mask the channel area with photoresists and oxygen plasma etching. IV characteristics of GRFETs are acquired in a probe station with a semiconductor parameter analyzer (4200-SCS, Keithley) in the ambient environment and in vacuum ($<1 \times 10^{-5}$ torr).

For this study, we investigated the effect of polymer passivation on either bottom or top surface of graphene. We applied passivation on the same device to compare the effect directly as describe below. For the bottom passivation, we utilized the whole device transfer method as previously demonstrated [34] to investigate the passivation effect on the same device. The process is described in Fig. 1. GRFETs are first fabricated on a Si/SiO₂ substrate and their device characteristics are obtained as explained before. For this study, we prepared three target substrates with different properties. One is a bare Si/SiO₂ substrate which is immersed in a HF solution for 30 s, resulting in more hydrophilic surface [34]. Two other Si/SiO₂ substrates are prepared with spin-coated polymers, one with PVA and the other with PDMS. After the fabrication and characterization of as-fabricated GRFETs, PMMA is spin-coated on the whole device and cured. Then, the whole device can be released from the substrate by etching SiO₂ layer with BOE solution with PMMA as a carrier layer. The transfer to any target substrate can be accomplished by fixing the device with a carrier layer onto a target substrate and removing PMMA with acetone as shown in Fig. 1.

For the top passivation, desired polymers (PVA, PDMS or stacks of both) are spin-coated and cured after GRFETs are fabricated and fully characterized. In these ways, we could compare the device characteristics of *the same* GRFETs before and after passivating bottom or top surface of graphene with desired polymers.

3. Results and discussions

Fig. 2 compares transfer characteristics [source-drain current (I_{DS}) vs. gate voltage (V_G)] of as-fabricated GRFETs on Si/SiO₂ substrate with those after they are transferred to new (passivated) substrates as described in Fig. 1. The transfer characteristics are all measured in vacuum to minimize p-type doping and hysteresis in the ambient condition. However, intrinsic p-type doping due to polymer residue and hysteresis associated with hard-to-remove water (such as trapped underneath graphene) are still unavoidable even in vacuum as can be seen in Fig. 2. In Fig. 2(a), a GRFET is transferred to a different Si/SiO2 surface with the same SiO2 thickness. The target substrate was briefly (30 s) etched in HF solution to make it more hydrophilic. After transfer, the GRFET shows reduced hysteresis and improved mobility as its electron mobility increases from 1300 cm²/V·s to 1900 cm²/V·s. In this work, electron field effect mobility, μ is calculated for downward sweeping direction of the gate voltage using $\mu = (L/W) (g_m/C_G V_{DS})$, where L and W are the length and width of the graphene channel, $C_{\rm G}$ is the gate capacitance, V_{DS} is the drain-source voltage, and g_{m} is the transconductance of the device. On the other hand, the charge (CNP) neutrality point remains almost the same $(V_{CNP} = ~14 \text{ V} - ~17 \text{ V}, V_{CNP} \text{ is determined by the average of two})$ CNPs, which depends on the gate voltage sweeping direction). As the target surface was briefly etched with HF, we expect more uniform or less electron-hole puddles on the surface compared to the original substrate, which may result in the better device characteristics since the minimum conductivity and mobility of graphene is strongly influenced by long range and short range



Fig. 1. A schematic for the "Cut & Paste" device transfer process [34]. After GRFETs are fabricated on a typical Si/SiO₂ substrate, they can be transferred to a target substrate with different surface properties. PMMA is used as a carrier layer similarly to graphene transfer process while SiO₂ acts as a sacrificial layer in this case. GRFETs which are adhered to PMMA can be released from the surface by etching SiO₂ with BOE and be transferred to prepared target substrates as a whole. More descriptions are given in the main text.

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