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Carrier transport through the ultrathin silicon-oxide layer in tunnel oxide passivated contact (TOPCon) c-Si solar cells

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ABSTRACT

The carrier transport through the silicon-oxide (SiO_x) layer in tunnel oxide passivated contact (TOPCon) c-Si solar cells has been studied experimentally and by simulation. The current intensity versus voltage (J-V) characteristics of GaIn/n-c-Si/SiO_x/n^+-poly-Si/Al structures shows a linear Ohmic characteristic, while a non-Ohmic behavior is observed in the samples without the n^+-poly-Si contact layer. Conductive Atomic Force Microscopy (c-AFM) images reveal some current spikes on the surface of the samples, which could be related to the transport through pinholes. The simulation results show that 1) a rectification characteristic is obtained when only the tunneling mechanism is included, 2) both the reverse saturation current and the forward current increase when a small amount of transport through pinholes is introduced, and 3) finally a linear Ohmic behavior is observed when the pinhole transport component reaches a certain level. Furthermore, the simulation for whole TOPCon solar cells provides some useful results. For very thin SiO_x (< 1.2 nm), the tunneling provides sufficient high tunneling probability and high efficiency TOPCon solar cells can be obtained without transport through pinholes if the passivation is ensured; while for a relatively thick SiO_x (> 1.2 nm) without the transport through pinholes, the TOPCon solar cell shows a poor fill factor (*FF*) with a high series resistance (*Rs*) because the tunneling does not provide a sufficient high transport channel for carrier transport, and the introduction of a small number of transports through pinholes improves the *FF* and reduces the *Rs*, hence improves the PCE. However, a high possibility for carrier going through pinholes reduces all of the performance parameters and degrades PCE for all the cases simulated. Therefore, an optimized pinhole density and size distribution is critical engineering for solar cell performance optimization. However, the establishment of an optimized method to precisely control the pinhole formation and characterization is still on the way.

1. Introduction

Crystalline silicon (c-Si) solar panels have been dominating the photovoltaic (PV) market since the PV technology become a viable renewable energy source because of the well-developed manufacturing technology with low manufacturing cost, abundant environmentally friendly raw materials, and high-level market acceptance. With the manufacturing technology improvements, the solar cell efficiency has been increased steadily in recent years, especially with some new cell structures introduced to replace the conventional p-type polycrystalline silicon (poly-Si) solar cells with an aluminum back surface field (ABF). Among them, the passivated emitter rear contact (PERC) solar cells have been developed and established a 25.0% world record efficiency in the 90's [1,2]. The PERC technology has been widely incorporated into large volume PV module productions in the PV manufacturing mainstream. Silicon Heterojunction solar cell with Intrinsic amorphous silicon (α-Si:H) Thin-layers (HIT) was also introduced in the 90's and has been proven to be a high efficiency (25.1%) solar cell structure with high open-circuit voltage (V_{oc}) up to 750 mV [3–5]. The combination of the HIT with the Inter-digitized Back Contact (IBC) has resulted in a new world record efficiency of 26.7% [6,7]. In recent years, the HIT technology has been transferred from laboratory to manufacturing in

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several companies. Because of the effective α-Si:H passivation, HIT solar cells have shown several advantages over PERC solar cells such as high V_{oc}, low temperature coefficient, and low manufacturing temperature. However, the manufacturing cost of HIT solar modules is still higher than that of PERC modules because of the low compatibility with the traditional silicon PV manufacturing process and the requirement for unique materials such as low temperature silver paste. To take the HIT advantages in the surface passivation and overcome the manufacturing non-compatibility issue at the same time, a new cell structure with a thin silicon oxide (SiO_x) surface-passivating layer and a doped poly-Si carrier collection contact was proposed. This new structure is named as TOPCon solar cell by taking the abbreviation of Tunnel Oxide Passivating Contact with the assumption of carrier transport through the ultrathin SiO_x (< 2.0 nm) by quantum tunneling [8–10]. The efficiency of TOPCon solar cell has been improved rapidly, and a 25.8% efficiency has been obtained without the IBC contact [11], which is higher than the 25.1% achieved by the HIT structure without the IBC contact [5].

Although the TOPCon cell efficiency has been improved quickly, some fundamental device physics has not been fully understood yet. An example is the carrier transport in the TOPCon structure. It is well known that SiO_2 is a perfect insulator and has been widely used as the insulating dielectric layer in Thin Film Transistors (TFT) in displays [12,13]. It is also an excellent surface passivation layer on c-Si for solar cell application. However, in TOPCon solar cells, photo-generated carriers have to transport through the insulating SiO_x layer, and the transport mechanism is logically assumed to be tunneling. On the other hand, because the SiO_x is very thin and pinholes could easily form during the SiO_x fabrication and/or thermal treatment. Therefore, one has proposed that the carrier transport could be through the pinholes in the SiO_x layer [14–18]. Experimentally, pinholes or weak SiO_x areas are indeed observed by cross-sectional transmission electron microscopy (TEM) [15] and scanning electron microscopy (SEM) on the surface of TOPCon structure with etching back of the doped poly-Si layer [16,17]. Also, current spikes were observed by conductive atomic force microscopy (c-AFM) [14], which could be considered as the evidence of carrier transport through pinholes. These experimental results confirmed the existence of pinholes in the SiO_x passivation layer and carriers could pass through the pinholes in principle. Recently, a temperature dependence dark current density versus voltage (J-V) study by Feldmann et al. [18] suggested that although transport through pinholes exists, the dominant transport is still going through tunneling. Then, the remaining question is how the carrier transport through pinholes affects the cell performance. In a simple word, are pinholes beneficial or harmful for TOPCon solar cell performance?

The objective of this paper is to experimentally identify the existence of pinholes in the SiO_x layer used in high-efficiency TOPCon solar cells and to study the carrier transport mechanisms in the SiO_x layer. In addition, we use a simulation to study the property of transport through pinholes and its effect on the cell performance. The dark J-V and c-AFM measurements confirmed that a portion of carrier transports is through pinholes; the simulation results showed that a proper amount of carrier transport through the pinhole benefits for the TOPCon solar cell performance for the SiO_x of and thicker than 1.0 nm, while too much carrier transport through pinholes degrades the cell performance by a noticeable reduction in all of the performance parameters.

2. Experimental details and simulation

The samples for the dark current-voltage (I-V) measurements were made on commercially available 0.2–2 Ω cm 170-μm n-type Cz c-Si wafers. The sample preparation involved surface damage removal with 25% tetramethylammonium hydroxide (TMAH) solution at 85 °C, followed by RCA chemical cleaning and SiO_x tunnel silicon oxide (SiO_x) growth in 68 wt% HNO_3 acid at 110 °C for 15 min. The resulting tunnel SiO_x thickness was ~1.4 nm, determined by spectral ellipsometry.

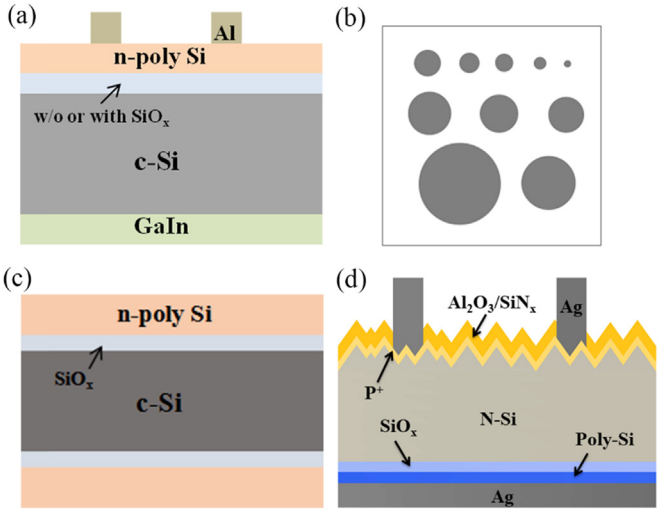

Fig. 1. Schematic drawings of (a) the layer structure of the sample for transport measurements, (b) electrode distribution for the I-V measurements, (c) layer structure of the samples for the passivation measurements, and (d) the TOPCon solar cell structure.

Next, a 40 nm thick phosphorus-doped hydrogenated amorphous silicon (n^+-α-Si:H) layer was deposited on one side using a plasma enhanced chemical vapor deposited (PECVD), followed by an 820 °C annealing for 30 min in an inert atmosphere to facilitate crystallization and dopant activation to turn the n^+-α-Si:H into n^+-poly-Si. After annealing, the front side metal contacts was realized by thermally evaporated Al dots through a shadow mask with various circular openings for different electrode areas and the back electrode was covered by GaIn to form an Ohmic contact with the n-type c-Si wafer. The sample structures were GaIn/n-c-Si/SiO_x/n^+-poly-Si/Al and GaIn/n^+-c-Si/SiO_x/Al, as described in Fig. 1(a), (b). Similarly, the samples for the minority carrier lifetime (τ) measurements were made with the same SiO_x and n^+-poly-Si fabrication process on both sides of the wafers but without the metal contact as shown in Fig. 1(c). The dark I-V characteristics were measured by a Keithley-4200 multi-function meter at the room temperature. The lifetime of the samples with different passivation layers were measured using a Sinton (WCT-120) system and the single-side reverse saturated recombination current density (J_0) and implied open-circuit voltage (iV_{oc}) were extracted from the measured photoconductive decays. The crystalline structure of the n + -poly-Si layer was measured using a Raman spectroscopy (Renishaw inVia-reflex) with 325 nm excitation laser to ensure the laser only probes the coating layer and the influence from the substrate c-Si wafer is minimized. The active phosphorus profile in the TOPCon structure was determined using an electrochemical capacitance-voltage (ECV) system (Buchanan, CVP21).

The TOPCon solar cells fabricated within this study have a designated area of 2 cm × 2 cm and are made of 0.2–2 Ω cm 170-μm n-type Cz c-Si wafers. The solar cell structure is shown in Fig. 1(d). The front side of the solar cells features an alkaline textured (random-pyramids) surface with a boron-doped p^+ emitter (80 Ω/□). Next, the ~1.4 nm tunnel oxide and the 40 nm n^+ poly-Si layers were grown on the rear side according to the process described above. Then a thin Al_2O_3 was deposited by atomic layer deposition (ALD) and a capped SiN_x:H film was deposited by PECVD for front surface passivation and anti-reflection coating. The rear-side full-area electrode was fabricated by thermally evaporated Ag; the front-side grids were realized by lithography technology cooperating with an e-beam evaporated Cr/Pd/Ag seed layer and then thickened by electroplating. The solar cell performance was characterized by one-sun light J-V measurements under a Class AAA solar simulator (Oriel, Sol3A) under AM 1.5 illumination (100 mW/cm^2) at 25 °C.

C-AFM imaging [19–21] was based on the contact mode of AFM