

## Avoiding blistering in Al<sub>2</sub>O<sub>3</sub> deposited on planar and black Si

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### ABSTRACT

Aluminum oxide (Al<sub>2</sub>O<sub>3</sub>) fabricated by atomic layer deposition (ALD) has during the last decade emerged as an excellent surface passivation material for both planar and micro/nanostructured silicon. The post-ALD thermal treatment required to activate the surface passivation of Al<sub>2</sub>O<sub>3</sub> results often in blistering and film delamination. Here, we studied how several fabrication steps affect blistering and the quality of surface passivation by Al<sub>2</sub>O<sub>3</sub>. Decreasing the fraction of blistered area on planar Si surfaces results in lower surface recombination velocity, in agreement with previous reports. By using simple analytical expressions, we estimated that surface recombination is at least 20 times faster at the blisters than at the non-blistered areas. Exposing the Si surface to a reactive ion etch (RIE) treatment as short as 30 s is enough to suppress blistering. Anti-reflective nanostructured Si (black Si) fabricated using the same RIE process by increasing the RIE time does not suffer from blistering either. Finally, we investigated the effective lifetime of black Si textured surfaces and we implemented a pre-ALD conditioning routine that dramatically improves the quality of passivation by Al<sub>2</sub>O<sub>3</sub> on black Si.

### 1. Introduction

The power conversion efficiency of silicon (Si) solar cells is severely affected by charge recombination at the surface of Si wafers, which mainly results in a less-than-ideal open circuit voltage [1,2]. Surface passivation is the act of decreasing surface recombination, typically performed by growing or depositing a thin dielectric layer on the surface of Si [3]. Aluminum oxide (Al<sub>2</sub>O<sub>3</sub>) has emerged as excellent material for passivation of Si, with performance comparable to or higher than that of thermally grown Si oxide (SiO<sub>2</sub>) [4]. Low surface recombination velocity has been achieved by depositing Al<sub>2</sub>O<sub>3</sub> by sputtering [5,6], plasma-enhanced chemical vapor deposition (PECVD) [7–9], and atomic layer deposition (ALD) [10–13]. Al<sub>2</sub>O<sub>3</sub> and Al<sub>2</sub>O<sub>3</sub>/SiN<sub>x</sub>:H stacks are already industrially relevant for: (i) rear side passivation of cells based on p-type substrates [14], thus replacing the traditional Al back surface field, and (ii) passivation of p<sup>+</sup> emitters in cells based on n-type substrates [15,16]. Al<sub>2</sub>O<sub>3</sub> has also demonstrated outstanding passivation performance when deposited on nanostructured, naturally antireflective Si (usually referred to as black Si [17], hereinafter bSi) [18,19]. The characteristic dimension of nanostructures in bSi leads to suppression of optical reflectance at the air-Si interface [20]. This in turn relaxes requirements on the antireflective properties of passivation films. If leading to enhanced photon absorption as compared to conventional texturing, higher short circuit current may also be obtained [21]. In addition, it has been shown that reflection off cells

based on bSi surfaces is less affected by the increase in incidence angle, which is particularly relevant for building-integrated applications [22,23]. bSi suffers from higher surface recombination given the increased surface area and the sub-surface damage originated by the texturing process (the latter when fabricated by reactive ion etch – RIE) [24], leading to losses in terms of open circuit voltage and fill factor. However, the gap between efficiency of bSi based cells and that of conventionally textured cells under same fabrication conditions is progressively closing [16], and the best passivation of bSi has been achieved so far by ALD coating with Al<sub>2</sub>O<sub>3</sub> [25].

A post-ALD thermal treatment in inert or slightly reducing atmosphere is mandatory to activate the passivation by Al<sub>2</sub>O<sub>3</sub> [4]. After such treatments, blistering is very often observed at the Si-Al<sub>2</sub>O<sub>3</sub> interface, sometimes leading to partial delamination of the Al<sub>2</sub>O<sub>3</sub> film [26–28]. Possible explanations put forward to explain formation of blisters are cavitation of the substrate caused by the surface diffusion of Si atoms, followed by buckling of the Al<sub>2</sub>O<sub>3</sub> after a critical internal pressure is reached [29–31] and mechanical shear stress due to thermal mismatch between Si and Al<sub>2</sub>O<sub>3</sub> during annealing [32]. The presence of SiN<sub>x</sub>:H as capping layer does not seem to avoid blistering [33], which is also found on surfaces textured by KOH (i.e. pyramid textured surfaces) [32]. While Vermang et al. showed that it is possible to exploit the presence of blisters to create local openings at the rear of a cell during contact firing [34], it is generally believed that blistering should be avoided if possible, in order to have a better control of the rear

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passivation. In addition, the quality of passivation of  $\text{Al}_2\text{O}_3$  is likely to be affected by the presence of blisters. A few studies reported variations of effective surface recombination velocity ( $S_{\text{eff}}$ ) with varying amount of blistering [32,35], based on effective lifetime ( $\tau_{\text{eff}}$ ) measurements using the quasi-steady state photoconductance method, and therefore averaged on full size wafers. In addition, experimental direct evidence that the local quality of the passivation is degraded at the blisters is difficult to obtain, although such an effect is expected. Several strategies have been employed to reduce blistering at the Si/ $\text{Al}_2\text{O}_3$  interface, including: decreasing the  $\text{Al}_2\text{O}_3$  thickness [33]; depositing the  $\text{Al}_2\text{O}_3$  at higher temperature, or letting the temperature rise during ALD (i.e. thermal drift ALD) [36]; using  $\text{O}_3$  as oxygen precursor instead of  $\text{H}_2\text{O}$  [27]; depositing  $\text{Al}_2\text{O}_3$  on a hydrophilic surface such as a chemically grown  $\text{SiO}_2$  layer [26]; varying the post-ALD thermal treatment temperature [27]. In all these cases, decreased blistering was attributed to the lower content of hydrogen in the films and/or the facilitated effusion of hydrogen from the films. However, hydrogen is also known as an excellent passivation agent for both bulk and surface defects in Si, and treatment in atmospheres containing hydrogen are routinely used to reduce recombination in Si solar cells. It follows that the gain in surface passivation by avoiding blistering should not be counteracted by any decrease in passivation due to lower content of hydrogen.

Here, we investigated the effect of several fabrication steps (pre-ALD cleaning, ALD temperature, post-ALD thermal treatment) on blistering and on the quality of surface passivation offered by  $\text{Al}_2\text{O}_3$  films. Based on electron microscopy images to determine the surface coverage of blisters and on a simple analytical model, we estimated the local recombination velocity at the blisters  $S_b$ , and we found that it is at least 20 times higher than that of the non-blistered areas. We found that exposing the Si surface to a 30 s reactive ion etch (RIE) treatment is enough to suppress blistering completely. Importantly, such a process does not increase  $S_{\text{eff}}$  within experimental deviations, and can be used as an alternative to the modifications to ALD and post-ALD processing that result in a lower content of hydrogen as side effect. We used the same RIE process to fabricate bSi textured surfaces, by increasing the RIE time, and we found that no bSi surfaces suffered from blistering either. Finally, we investigated the effective lifetime of bSi surfaces and the effect of pre-conditioning of the ALD chamber on the quality of the passivation by  $\text{Al}_2\text{O}_3$  on bSi.

## 2. Experimental section

### 2.1. Fabrication

100 mm diameter Czochralski (CZ) mono-crystalline (100) p-type boron-doped Si wafers with thickness  $525 \pm 25 \mu\text{m}$  or  $350 \pm 25 \mu\text{m}$  and resistivity of  $5 \Omega\text{cm}$  were used as substrates. Some wafers were textured on one side using mask-less reactive ion etch (RIE) at  $-20^\circ\text{C}$  in a Pegasus system (SPTS) using the following parameters: 3000 W coil power, 10 W platen power (both operating at 13.56 MHz), gas flow ratio  $\text{O}_2$ :  $\text{SF}_6 \approx 10:7$ , chamber pressure of 34 mTorr. The etching time varied from 30 s to 16 min depending on the wafer. All wafers were then RCA (Radio Corporation of America) cleaned (RCA1: 1:1:5 mixture of  $\text{H}_2\text{O}_2$ ,  $\text{NH}_4\text{OH}$  solution and de-ionized water; RCA2: 1:1:5 mixture of  $\text{H}_2\text{O}_2$ , HCl solution and de-ionized water; both solutions were heated to  $70^\circ\text{C}$ ). For some wafers, the final oxide strip in 5% diluted hydrofluoric acid (HF) was omitted, in order to keep the  $\text{SiO}_2$  from the second part of the cleaning on the surface. The surfaces were passivated with 380 cycles of  $\text{Al}_2\text{O}_3$  synthesized at 200 or  $250^\circ\text{C}$  in an atomic layer deposition (ALD) process (R200, Picosun). Trimethyl-aluminum (TMA) and  $\text{H}_2\text{O}$  were used as precursors for aluminum and oxygen, respectively. In some cases, a chamber preconditioning procedure was employed where 50 cycles were deposited on the wafer holder without any wafer in the chamber. The  $\text{Al}_2\text{O}_3$  layers were activated by post-deposition treatment. Some wafers were annealed in a  $\text{N}_2$  atmosphere using a Tempress furnace. Annealing temperature was either  $400^\circ\text{C}$  or

$500^\circ\text{C}$ , and the annealing time was either 10 or 30 min. The other wafers received a rapid thermal annealing at  $400^\circ\text{C}$  or  $500^\circ\text{C}$  in a Jipelec RTP tool. The ramp-up time, annealing time and ramp-down time were 1 min, 5 min and 1 min, respectively.

### 2.2. Characterization

The thickness of the  $\text{Al}_2\text{O}_3$  layer was measured using ellipsometry (VASE J. A. Woollam Co.). Scanning electron microscopy (SEM) images were acquired using a Carl Zeiss Supra 40VP microscope at an acceleration voltage of 5 kV. Size and surface coverage of the blisters were calculated from top-view SEM images using the image analysis software ImageJ. Optical reflectance  $R$  and transmittance  $T$  were measured using a UV spectrophotometer (UV-2600, Shimadzu Co.). The absorbance  $A$  was then determined using the relation  $A = 1 - R - T$ . Effective lifetime measurements were performed using the microwave-detected photoconductivity (MDP) method in transient single point and mapping mode, at an injection level  $\Delta n$  of  $\sim 10^{15} \text{cm}^{-3}$ , using a MDP mapper (Freiberg Instruments). For symmetrical, non-textured wafers, the effective surface recombination was calculated using the relation  $S_{\text{eff}} = W/(2\tau_{\text{eff}})$ , where  $W$  is the wafer thickness and  $\tau_{\text{eff}}$  is the effective lifetime.  $S_{\text{eff}}$  was then used to calculate the surface recombination velocity of the textured surface according to the relation:  $S_{\text{textured}} = W/\tau_{\text{eff}} - S_{\text{planar}}$ .

## 3. Results and discussion

### 3.1. Blistering in $\text{Al}_2\text{O}_3$ on flat Si

We fabricated a first set of wafers to test the effect of ALD deposition temperature and furnace annealing on formation of blisters on surfaces which have been cleaned following the complete RCA procedure, including the final oxide strip using 5% diluted HF. The  $\text{Al}_2\text{O}_3$  thickness was fixed to 30 nm. Previous work using our ALD reactor, as well as by other groups [18,37], indicated that such thickness is required to passivate bSi well. We chose ALD deposition temperatures of 200 and  $250^\circ\text{C}$ , since these temperatures usually define the window resulting in higher quality of passivation [4]. We followed the same reasoning for the post-ALD annealing temperature,  $400^\circ\text{C}$  or  $500^\circ\text{C}$ . We annealed the wafers for 30 min and 5 min at  $400^\circ\text{C}$  and  $500^\circ\text{C}$ , respectively, so that all wafers would remain in the furnace for approximately the same time. This is because the idle temperature of the furnace is  $400^\circ\text{C}$  and the ramp-up and ramp-down time for the process is of  $10^\circ\text{C min}^{-1}$ . Fig. 1 shows top-view low magnification SEM images of 4 wafers with

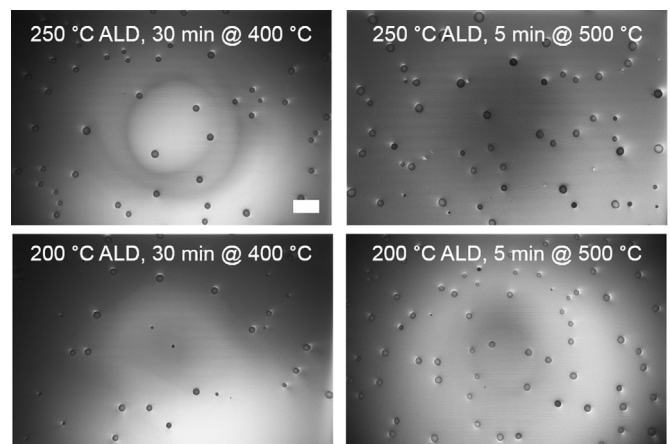


Fig. 1. Top-view, small magnification SEM images of flat wafers after RCA cleaning (including last HF dip),  $\text{Al}_2\text{O}_3$  deposition and annealing in a tube furnace. Blistering is critical on these wafers, with diameter up to around  $100 \mu\text{m}$ . The scale bar represents  $200 \mu\text{m}$ .

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