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monoPoly[™] cells: Large-area crystalline silicon solar cells with fire-through screen printed contact to doped polysilicon surfaces



Shubham Duttagupta*, Naomi Nandakumar, Pradeep Padhamnath, Jamaal Kitz Buatis, Rolf Stangl, Armin G. Aberle

Solar Energy Research Institute of Singapore (SERIS), National University of Singapore (NUS), 117574 Singapore, Singapore

ABSTRACT

Successful integration of carrier selective contacts (so-called passivated contacts) in *p*-type and *n*-type front-and-back contact (FAB) silicon solar cells could lift cell efficiencies to above 24% in mass production. In this work, we introduce one of SERIS' monoPoly FAB cell structures, which features the monofacial (single-sided) application of a polysilicon (poly-Si) layer. Using industrial tools, doped poly-Si on an ultrathin interface oxide is shown to provide extremely low recombination current density of 4 fA/cm² and implied open-circuit voltage of about 745 mV that are able to withstand the high-temperature firing process of screen-printed metal contacts. The interface oxide and the doping concentration of the poly-Si film are of great importance for the surface passivation quality and the transport of majority carriers, especially for fire-through screen-printed contacts as used in this work. Our initial pilot-line results show a very promising cell efficiency of 21.4% on large-area (244.3 cm²) *n*-type monocrystalline wafers with screen-printed and fire-through metal contacts on both sides. A roadmap for *n*FAB monoPoly cells towards 24% efficiency is presented on the basis of an optimisation of the device architecture and various processing steps.

1. Introduction

Global photovoltaic (PV) production continues to be dominated by *p*-type crystalline silicon (*c*-Si) cell technologies [1]. Despite continual improvements in screen-printed passivated emitter and rear cells (PERC), it is apparent that the path towards even higher commercial device efficiencies (> 22%) must be through the use of more advanced processes, as evidenced by the monocrystalline silicon efficiency records achieved in recent years [2–6]. The use of *n*-type Czochralski (Cz) substrates seems advantageous as these wafers feature higher bulk lifetimes than *p*-type Cz wafers and could enable higher open-circuit voltages (*V*_{OC}) and thus provide a path towards higher efficiency. *n*-type devices are believed to have the additional advantage of being unaffected by the light-induced degradation problem caused by boronoxygen complexes [7]. It is for these reasons that the ITRPV predicts that *n*-type *c*-Si devices will account for > 25% of global PV production by 2027 [1].

In SERIS, front-and-back contact (FAB) cells are referred to as *n*FAB or *p*FAB cells, depending on the polarity of the substrate (*n*-type or *p*-type). These structures can be monofacial or bifacial. Until mid-2017, the best fully screen-printed commercial *n*-type *c*-Si cells had efficiencies of about 21%, using H-patterned contacts on both sides and a homogenous emitter and phosphorus-doped back-surface field (BSF), the latter achieved either with thermal diffusion or with ion implantation. Progress towards higher efficiencies (> 24%) in mass

production will likely come from suppression of recombination at the front and, particularly, the rear c-Si surfaces, including recombination losses at the metal-silicon contacts. Passivated contacts using doped poly-Si have recently gained considerable interest as a possible solution to this problem [5]. An interface oxide (iOx) layer separating the silicon absorber and the contact system appears to be the mandatory ingredient for ultra-high efficiency silicon solar cells, as used for many years in heterojunction cells [2,3] and, very likely, also in SunPower's interdigitated back contact cells [4], although none of these cells uses high-temperature fire-through contacts. The metal-insulator-semiconductor (MIS) solar cells [8,9] also used a thin insulator between the semiconductor and the metal in order to reduce recombination losses, while retaining charge carrier selectivity. The introduction of passivated contacts to high-volume screen-printed solar cell manufacture is, hence, very appealing and at the same time challenging. It requires the passivated contact to be thermally stable when metallized with an industrial screen-printing process that includes commercially available fire-through pastes. It also requires high-throughput and low-cost deposition schemes for the passivated contacts preferably with minimal additional process steps, for example with single-side deposition and multi-layer deposition within a single system.

Although there is a large variety of materials that can be implemented in a carrier-selective passivated contact (see the summary in Ref. [10]), one combination which has demonstrated successful results is an ultrathin (1-2 nm) silicon oxide (SiO_x) iOx layer capped by an *n*-

* Corresponding author.

E-mail address: shubham.duttagupta@nus.edu.sg (S. Duttagupta).

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Fig. 1. Schematic of an *n*-type bifacial monoPoly silicon solar cell structure with an electron-selective passivated contact at the rear.

type (phosphorus-doped) polycrystalline silicon layer [hereafter referred to as poly-Si (n^+)] for large-area fire-through screen-printed contacts [11]. Interface oxide films can be grown using several methods, usually wet chemically [12–15], by thermal oxidation, or by ALD [16,17]. SERIS' monoPoly FAB cell structure features polysilicon (poly-Si) contacts at the front or at the rear side of the *c*-Si substrate that can be either electron or hole-selective. The emitter could be either at the front or at the rear side. The cell structure with bifacial polysilicon (poly-Si) contacts is referred to as biPoly FAB cell (not presented in this paper). The substrates can be either multicrystalline or monocrystalline wafers with either *n*-type or *p*-type polarity. An example for a monoPoly FAB cell with front boron emitter and rear-side poly-Si (n^+) contact, as investigated in this work, is shown in Fig. 1. In this paper, we report our

initial results on SiO_x iOx layers grown in-situ by a low-pressure chemical vapour deposition (LPCVD) process. monoPoly solar cell results achieved in SERIS' R&D pilot cell line are then presented, followed by a roadmap towards 24% monoPoly cell efficiency in mass production.

Fig. 2 shows examples of process flows used for the fabrication of classical nFAB cells and monoPoly FAB cells using *n*-type or *p*-type substrates and a poly-Si layer at the rear. Process flow A is a simple bifacial *n*FAB process with a homogeneous emitter and a homogeneous BSF - based on the so-called Passivated Emitter and Rear Totally Diffused (PERT) structure - with merely 8 steps. There are also ways to avoid the masking step, however, this is not part of the scope of this paper. This cost-effective *n*FAB cell with commercial material (wafer material, pastes) properties available today has an efficiency potential of about 21.5% with a homogeneous emitter and BSF, each having a screen-printed H-pattern electrode with 5 busbars. Recombination at the rear n^+ -BSF (both passivated and metal-contacted regions) and within the n^+ layer is the main limiting factor that prevents this cell structure from reaching very high efficiencies (i.e. > 22%). Process flows B and C introduce iOx and hydrogenated poly-Si layers at the rear side that can significantly reduce overall recombination and at the same time maintain good majority carrier transport. The main difference between B and C is the method of deposition. B uses a tube-based LPCVD process, while C uses a single-sided PECVD process. Another difference is the need for a mask and an alkaline wet-chemical step to etch polysilicon wrap-around in process flow B, which is not needed in process flow C. The poly-Si layers can be in-situ doped or ex-situ doped (diffused or implanted), based on manufacturers' preferences.

2. Experimental details

SERIS' *c*-Si photovoltaic R&D focuses on large-area (6 in. - M0, M1, M2 and M4 sizes) *p*- and *n*-type Si wafers as used by solar cell manufacturers in high-volume production. In this work, we report our initial results using process flow B of Fig. 2. We limit the results to process B mainly due to page restrictions. *n*-type (170 μ m, 2 Ω cm, < 100 >) Cz



Fig. 2. (A) Simple process flow to fabricate SERIS' bifacial nFAB cells. Presently, such cells have about 21.5% efficiency potential in mass production, with a homogeneous emitter and a homogeneous BSF. (B) Preliminary process flow at SERIS to fabricate monoPoly FAB cells with a rear poly-Si layer deposited by a LPCVD process. (C) Preliminary process flow at SERIS to fabricate monoPoly FAB cells with a rear poly-Si layer deposited with a 'single-sided' PECVD process. Process flows B and C are estimated to have efficiency potentials of 24% in mass production.

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