Solar Energy Materials and Solar Cells 186 (2018) 42–49

Contents lists available at ScienceDirect

Solar Energy Materials and Solar Cells

journal homepage: www.elsevier.com/locate/solmat

The influence of surface structure on diffusion and passivation in multicrystalline silicon solar cells textured by metal assisted chemical etching (MACE) method

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ARTICLE INFO

Keywords:
Metal assisted chemical etching
Multicrystalline silicon solar cells
Diffusion
Passivation

ABSTRACT

It is important to improve the efficiency of solar cells textured by the MACE method, and the surface morphology has a significant effect on the efficiency. In this paper, we textured multicrystalline wafer using MACE method, and the surface morphology was further modified by post-etching process to achieve high efficiency. The influence of structure on diffusion and surface passivation was studied. It reveals that surface structure has a big effect on diffusion and passivation, thus affecting the efficiency. Structure with large aspect ratio results in heavily doped regions and poor passivation performance. Finally, large area solar cells with the efficiency of 19.08% and 19.11% were obtained on slurry wire and diamond wire saw multicrystalline wafer respectively, which is 0.5% and 0.8% absolutely higher than the cells with traditional acid texturing.

1. Introduction

The PV (photovoltaic) market has seen rapid growth over the past decades. With the benefit of abundant resources and technology maturation, silicon (i.e. monocrystalline silicon(c-Si) and multicrystalline silicon (mc-Si)) solar cells accounts for about 90% in the total PV market share. There are many improvements in technologies such as the purification of silicon materials [1], crystal growth [2], and fabrication process optimization (diffusion, passivation and metallization) [3–5], all of which function together to achieve conversion efficiency of ~ 19% and ~ 18% respectively in c-Si and mc-Si respectively in commercial production line. In general, a new technology can result in a decrease in cost or increase in performance. Compared to slurry wire saw (SWS), diamond wire saw (DWS) can reduce the cost per piece of crystalline Si wafer by about 10%, but suffer a difficulty in texturing with traditional acid etching because of the reduced and non-uniform distributed surface defects. This disadvantage causes a delay in the application of DWS in mc-Si industry. However, there is no such problem in c-Si which using anisotropic etching method.

Metal-assisted chemical etching (MACE) method can form nano-pillar [6], nano-hole [7], porous silicon [8], and inverted pyramid [9] structure on crystalline silicon under certain conditions. Wafers with these structures have low surface reflectance and appear dark (or even black) and therefore referred to as 'black silicon'. Except for MACE, there are many other ways, such as laser treatment [10], reactive ion etching (RIE) [11], electrochemical etching [12], atmospheric pressure F_2 based dry etching [13], microwave and plasma texturing [14,15], PIII (plasma immersion ion implantation) [16–18] etc. to form black silicon structure. These methods also have the potential to achieve high efficiency on multicrystalline silicon wafer. Of the existing texturing methods, however, we believe that MACE has the best chances of industrialization mainly due to its low cost of ownership. In recent years, 'black silicon' has been applied to silicon solar cell to reduce surface reflectance. But in the earlier days, as-prepared 'black silicon' after cleaning was used to fabricate solar cell directly, which resulted in low efficiency because of high surface defect density [19,20]. Then, in order to improve the cell performance, post-process such as alkaline etching was used to adjust surface morphology and decrease defect density [21,22]. Nowadays, efficiency up to 18% can be realized on mc-Si by MACE method, but only several researches reported efficiency beyond 19% on mc-Si [23]. There were still difficulties in achieving high-efficient solar cell on mc-Si (especially on large scale) using MACE method.

In this paper, mc-Si was etched by MACE method, then was post

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https://doi.org/10.1016/j.solmat.2018.06.011
Received 18 February 2018; Received in revised form 21 May 2018; Accepted 6 June 2018
0927-0248/

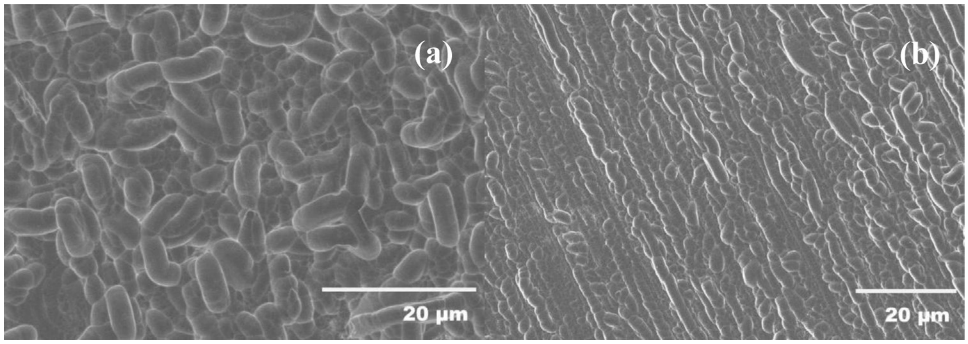

Fig. 1. SEM image of mc-Silicon wafer after acid texturing; (a) SWS wafer; (b) DWS wafer.

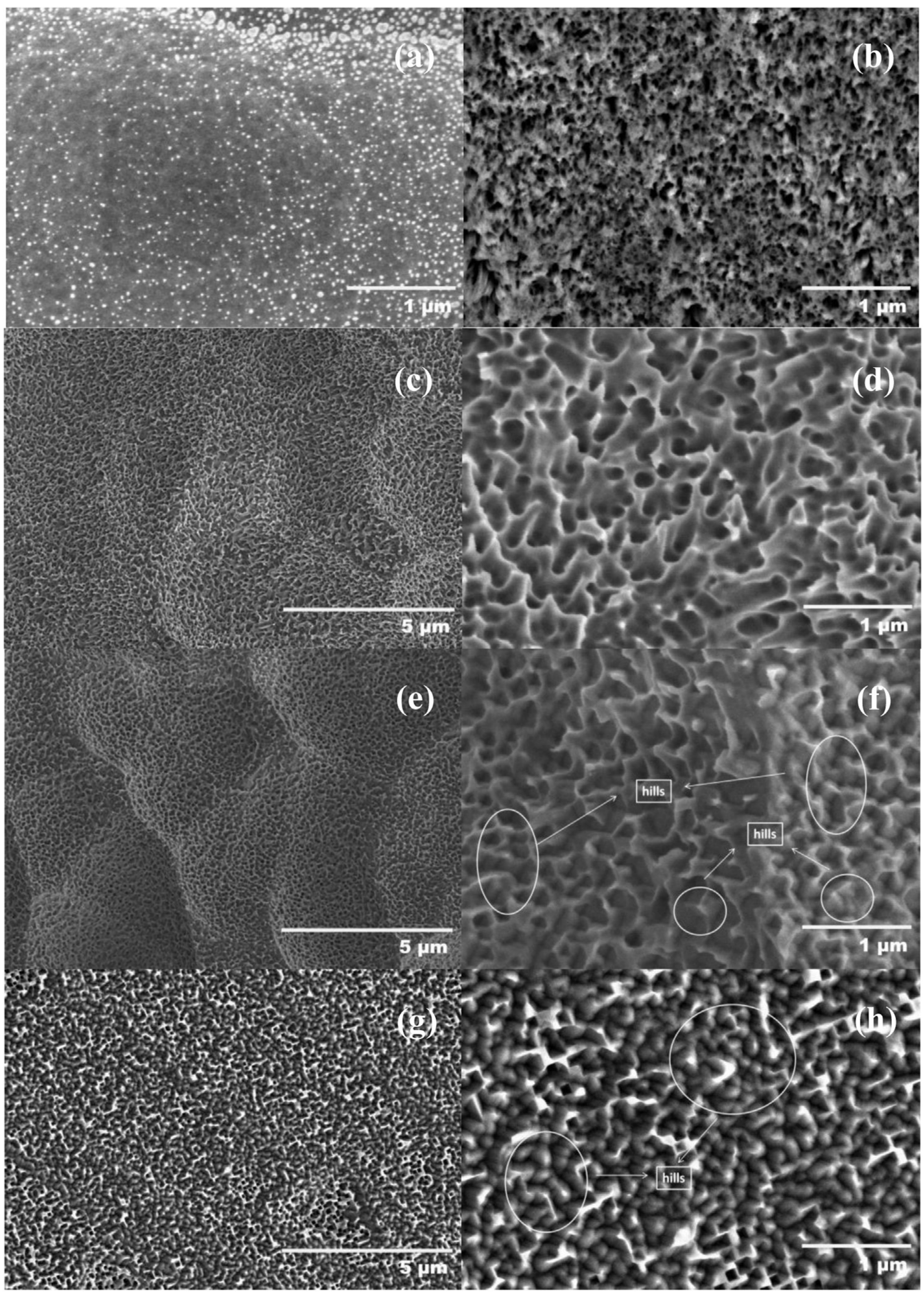

Fig. 2. SEM images of black silicon; (a) silver nanoparticles as deposited; (b) without PEP; (c) and (d) with PEP on SWS wafer, S60A60; (e) and (f) with PEP on SWS wafer, S90A60; (g) and (h) with PEP on DWS wafer, S90A60.