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21% efficient screen-printed *n*-type silicon wafer solar cells with implanted phosphorus front surface field

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ABSTRACT

In this paper *n*-type PERT (Passivated Emitter and Rear Totally diffused) silicon wafer solar cells with a diffused boron rear emitter and an implanted phosphorus front surface field are investigated. A key feature of the *n*-PERT rear emitter cell is that it uses the same sequence of surface passivation, rear local laser ablation and screen-printing processes as a commercial *p*-type PERC (Passivated Emitter and Rear Contact) cell. Therefore, this cell structure is very industrially relevant as it could simplify a production line upgrade from *p*-type cells to *n*-type cells. Additionally, ion implantation provides an elegant single-side doping process that further simplifies the processing sequence of *n*-PERT cells. Ion implantation also provides excellent control over the doping profile via a variation of post-implant annealing time. The effect of annealing time on the implanted phosphorus surface was evaluated in this study in terms of the front surface field dopant profile and its impact on the solar cells' electrical characteristics. A shallower front surface doping profile resulted in better short wavelength response. Additionally, the performance of two different Al pastes (with and without Si content in the paste) was compared. The better-performing Al-Si paste generates a homogeneous Al-p^+ region under the contacts, which reduces the recombination at the contacts. By tailoring the phosphorus front surface field profiles and by minimising the recombination during the rear Al contact formation, efficiencies of up to 21% on large area 244 cm^2 *n*-type wafers were achieved so far.

1. Introduction

Over the last few years, the photovoltaic (PV) industry has become increasingly interested in *n*-type Czochralski-grown silicon (Cz-Si) wafer solar cells due to their high efficiency potential. The International Technology Roadmap for Photovoltaics (ITRPV, 2017) predicts the market share of *n*-type Cz-Si wafer solar cells will be greater than 25% by 2027 [1]. The main reasons for the high efficiency potential of *n*-type c-Si wafers when compared to the industry dominant *p*-type c-Si wafers are the following: a) n-type c-Si wafers are less sensitive to metallic impurity contamination [2], and this makes it easier to maintain high lifetimes during the cell fabrication process [3,4]. b) *n*-type c-Si wafers do not suffer from light-induced degradation (LID), mainly caused by the boron-oxygen complexes [5,6]. As a consequence, most of the high-efficiency (> 24%) solar cell architectures use *n*-type c-Si wafers.

Aluminium back-surface field (Al-BSF), and passivated emitter and rear cell (PERC) are the two dominant solar cell structures in the PV market today associated with *p*-type c-Si wafers. Moving to *n*-type c-Si wafers allows to explore advanced high-efficiency solar cell architectures. Passivated emitter and rear totally diffused (*n*-PERT), passivated emitter and rear locally diffused (*n*-PERL), heterojunction (*n*-HJT), and interdigitated back contact (*n*-IBC) are some of the promising solar cell architectures that use *n*-type c-Si wafers. However, most of these advanced solar cell architectures are disruptive and require additional tool sets as compared to mainstream p-type technologies. The *n*-PERT rear emitter solar cell uses the same sequence of surface passivation, rear local laser ablation and screen-printing processes as p-type PERC solar cells (see Fig. 1 left). Therefore, this cell structure is very industrially relevant as it could potentially simplify a production line upgrade from *p*-type to *n*-type cells [7,8].

The *n*-PERT rear emitter solar cell depicted in Fig. 1 uses the same

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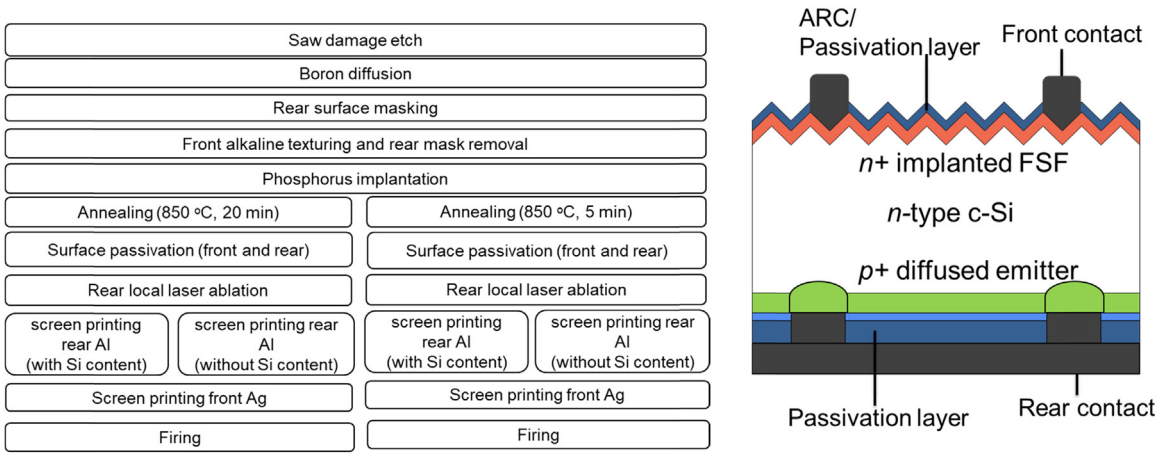

Fig. 1. Process flow for the fabrication of rear emitter *n*-PERT solar cell and the schematic of the solar cell fabricated in this work.

screen-printed metallisation processes as a PERC solar cell. This structure avoids the problems associated with the usage of Ag-Al pastes to contact boron-doped surfaces. A drawback of the Ag-Al pastes is higher metal recombination at the metal-Si interface, when compared to Ag pastes that are used to contact phosphorus-doped surfaces [9]. Screen-printed metallisation of textured phosphorus-doped surfaces is a well-established process [10]. Innovative Ag pastes have been developed to enable contacting phosphorus-doped surfaces with surface doping concentrations around or even less than 1×10^{20} active dopant atoms/cm^3 [11–13]. This improves both the open-circuit voltage (V_{oc}) due to reduced heavy doping effects and the short-circuit current (I_{sc}) due to improved blue response of the solar cells [14].

There are various reports in the literature on rear emitter *n*-PERT solar cells [4,6,8,15–18]. Until now, rear emitter *n*-PERT solar cells using BBr_3 and $POCl_3$ furnace diffusions in the fabrication process flow have demonstrated conversion efficiencies of up to 22.5% using Ni/Cu/Ag plating on the front side and AlSi sputtering on the rear side for metallisation [19] and with screen-printed metallisation process upto 21.9% [15]. In this study, *n*-PERT rear emitter solar cells using a rear boron diffusion and a front phosphorus ion implantation were fabricated. By using a single-side doping technique like implantation, the process sequence can be simplified, as it does not require additional sacrificial masking layer deposition and etching steps [20]. The impact of annealing phosphorus-implanted samples on the electrical characteristics of the *n*-PERT solar cells was studied. The phosphorus implanted front surface field (FSF) can significantly influence solar cell characteristics such as contact resistance, V_{oc}, and short wavelength response [21]. A shallower front surface field resulted in better short wavelength response and better efficiency values in this study. By tuning the phosphorus front surface field profile and by optimising the rear Al contact formation, cell efficiencies of up to 21.0% were achieved on large-area (244 cm^2) *n*-type Cz-Si wafer solar cells.

2. Experimental details

In this study, large-area (244 cm^2) *n*-type pseudo-square Cz-Si wafers with 3–5 Ω cm bulk resistivity were used. The wafers were saw damage etched, followed by a standard wet-chemical cleaning sequence: Radio Corporation of America (RCA) clean 1 and 2, followed by a dilute hydrofluoric acid (HF) dip. The wafers then went through a boron diffusion (sheet resistance of 100 Ω/sq, diffused on both sides of the wafers) process in an industrial tube diffusion furnace. Following the boron diffusion process, the borosilicate glass (BSG) layer was etched and the rear surface of the cells was coated with a 160 nm thick PECVD (plasma-enhanced chemical vapour deposition) silicon nitride (SiN_x) mask (MAiA, Meyer Burger, Germany). This acts as an etching barrier for the subsequent alkaline texturing process. The wafers were textured using an IPA (isopropyl alcohol)-free alkaline texturing solution, to generate random pyramid surface texture on the front surface of the wafer. After the removal of the rear masking layer (using HF), the wafers were phosphorus-implanted on the front side using an industrial ion implanter. The wafers were then split into 2 different groups and annealed at 850 °C for either 5 min or 20 min. This resulted in FSF sheet resistances of 115 Ω/sq for the 5 min anneal group, and 95 Ω/sq for the 20 min anneal group.

The rear side of the wafers was passivated using a stack of PECVD aluminium oxide-silicon nitride (AlO_y-SiN_x) with a thickness of 40 nm and 100 nm respectively, and the front side was passivated with PECVD SiN_x (70 nm thick) using an industrial inline machine (MAiA, Meyer Burger, Germany). The rear AlO_y-SiN_x stack was then locally ablated using a nanosecond (ns) green laser (Innolas Solutions, Germany) with a pulse duration of 38 ns. At this laser-operating wavelength, the dielectric is transparent, and the energy of the laser is hence absorbed in the underlying silicon surface (boron-diffused emitter). As a result, the silicon melts locally and lifts off the dielectric layer (indirect ablation) [22]. The boron-diffused emitter under the laser-opened regions is damaged because of this laser ablation process. An optical image of the laser opening on the rear dielectric layer is shown in Fig. 2. The dielectric was patterned with 45 μm diameter dots openings with a pitch of 400 μm. Following this Al was screen-printed onto the cell's rear surface. Two different Al pastes from Toyo (Japan) were used in this study (an Al paste without added Si and an Al paste with added Si). The Al paste is made with greater than 80% pure Al powder, whereas the Al-Si paste is made with 70–80% Al-Si atomized powder with Si content of 5–25%. For one batch of cells, the rear side was printed with the pure Al paste and for the other batch it was printed with Al-Si paste. The front grid (35 μm finger opening with 105 fingers and 5 busbars with a busbar width of 800 μm) for all cells was printed using the Ag paste PV 20 from DuPont. The cells were then fired at an optimised firing profile using an industrial fast firing furnace.

3. Results and discussion

3.1. Front surface field characterisation

The boron-diffused emitter and the implanted phosphorus front surface field layers were characterized using a 4 point probe to determine sheet resistance and an electrochemical capacitance-voltage profiler to determine the dopant profile. ECV measures charge carriers which is equal to the active dopants in the semiconductor. We applied a calibrated area factor to correct the ECV profiles of the textured surfaces and it was verified that the sheet resistance calculated from the profile matched the sheet resistance value measured via 4 point probe method within + / − 5%. The cells' implied V_{oc} was measured by