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Phosphorus diffused LPCVD polysilicon passivated contacts with in-situ low pressure oxidation

Kean Chern Fong[a,*], Teng Choon Kho[a], WenSheng Liang[a], Teck Kong Chong[a], Marco Ernst[a], Daniel Walter[a], Matthew Stocks[a], Evan Franklin[a,b], Keith McIntosh[c], Andrew Blakers[a]

[a] The Australian National University, Engineering Building, North Road, 2600 Canberra, Australia
[b] School of Engineering and ICT, University of Tasmania, Hobart 7001, Australia
[c] PV Lighthouse, Coledale, NSW 2515, Australia

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ABSTRACT

As silicon photovoltaic technology advances, charge carrier losses at the contacted interfaces of the silicon absorber are coming to dominate power conversion efficiency. The so-called passivated contact, which provides selective charge-carrier extraction while simultaneously reducing interface recombination, is thus of significant interest for next-generation silicon solar cells. However, achieving both low recombination and low resistance to charge carrier extraction has proven challenging. Here, we present a passivated contact technology based on polysilicon deposited using low pressure chemical vapour deposition (LPCVD) over an ultra-thin silicon dioxide layer, which achieves an excellent surface passivation with implied open-circuit voltage of 735 mV, a recombination prefactor below 1 fA cm^{-2} and contact resistivity below mΩ cm^2.

Key to this technology is the deposition of an ultra-thin silicon dioxide interlayer under high temperature and low pressure condition, performed in-situ within a single process with the polysilicon deposition. Additionally, the passivating contact structure maintains its electronic properties at temperatures of up to 900 °C and is compatible with existing industrial processes. The presented work therefore represents a significant advancement in industrially-applicable passivated contact technology.

1. Introduction

Significant advances have been made in the last few years in the area of doped polycrystalline silicon on interfacial oxide (Poly-Ox) as a passivated contact. The passivation quality has progressed tremendously, with recent reports of both p + and n + Poly-Ox contacts of approximately 1 fA cm^{-2} [1,2], and application of Poly-Ox technology to cell fabrication has demonstrated efficiencies over 25% [3,4].

Numerous methods of fabricating the Poly-Ox structure have proven successful at producing results applicable to high efficiency silicon solar cells. The interfacial oxide layer can be grown thermally in an oxygen ambient [5], or a wet chemical process [5–7]. The polysilicon layer can be deposited via PECVD or LPCVD, and in-situ doped with diborane or phosphine added into the deposition gas mix [1,5,8,9]. Alternatively, an intrinsic amorphous or polycrystalline silicon layer can be deposited which is then doped in a separate process via furnace diffusion [9–11] or ion implantation [12,13]. The films are temperature stable, and retain excellent surface passivation properties after very high temperature processing up to 950 °C [14], thus being highly compatible with industrial processes.

Application of passivated contacts to solar cells requires fulfilment of two key electrical requirements; having sufficiently low surface recombination and low contact resistivity. In the case of a full area rear contact cell, the surface passivation is the key property, and a high contact resistivity below 100 mΩ cm^2 is generally tolerable. However, Poly-Ox contacts are increasingly being explored for application under metal fingers to form local contacts in interdigitated back-contact (IBC) [14,15],bifacial solar cells [1] and passivated emitter rear contact solar cells (PERC) [1,15–18]. The small contact area necessitates lower contact resistivity in order to avoid high series resistance losses. However, investigation of polysilicon contacts, and other forms of passivated contacts in literature suggests that some trade-off between surface passivation and contact resistivity is inevitable, requiring careful optimisation for application to specific cell designs [10,19–22].

A significant advancement in passivated contact technology is presented, where very low surface recombination, and very low contact resistivity is achieved. Such contact films are therefore applicable to both full area contact and localized contact solar cells without the need

* Corresponding author.
E-mail address: kean.fong@anu.edu.au (K.C. Fong).

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for a trade-off in the electrical characteristics. The novelty of this work lies in the use of low-pressure (< 600 mTorr) thermal oxidation to control the growth conditions for the interfacial oxide grown at temperatures between 700 and 850 °C. Furthermore, as it is performed in-situ to the polysilicon deposition the oxide is not exposed to the atmosphere prior to be capped with polysilicon, allowing fine control of ultra-thin (< 1.5 nm) high quality oxide layer with high repeatability. The experimental details and excellent electrical properties of the film achieved with this technique are presented, along with discussions on the measurement methods, and observed correlation between electrical characteristics to the process conditions.

2. Materials and methods

Samples were prepared using 1 and 100 Ω cm phosphorus doped float-zone (FZ) wafers, which have been etched in tetramethylammonium hydroxide (TMAH) solution at 85 °C to remove surface damage, RCA cleaned, and pre-processed in a long oxidation anneal to eliminate vacancy related defects causing bulk lifetime reduction and formation of low lifetime regions in concentric circles as is typically seen in FZ wafers [23]. After defect annealing, the resistivity of the wafers were measured to be within 5% of the rated resistivity, and have a thickness of 385 ± 5 μm. The resistivity of the bulk material is assumed to be the rated resistivity for subsequent calculations of J_0 and contact resistance, ρ_c. The formed oxides were stripped in 10% hydrofluoric (HF) acid solution, and the samples were cleaned once again in RCA solution and etched in dilute HF acid immediately prior to being loaded into the LPCVD furnace.

Thermal oxidation for tunnel oxide growth was performed under low pressure conditions between 700 °C and 800 °C for times in the range of 5–15 min at a pressure of 600 mTorr. The furnace chamber was then evacuated prior to polysilicon deposition. An undoped polysilicon layer was deposited by filling the chamber with pure silane gas at 520 °C for 30 min. Both thermal oxidation and polysilicon deposition was performed within a single process using a Tempress LPCVD furnace. The thickness of the polysilicon layer is approximately 20 nm, as measured on films deposited using the identical recipe on a quartz wafer, measured by means of spectral ellipsometry using a JA Woollam M2000D [24]. Attempts to measure the interfacial oxide thickness using spectral ellipsometry proved difficult as we observed significant error in the fits to optical models for SiO_2 on Si wafers. Furthermore, the fitting suggesting thickness between 0 nm and 1 nm were arbitrary, and does not provide correlating trend to the oxide growth time and temperature. This is contrary to the clear correlation observed between oxidation time and temperature to the electrical behaviour such as sheet resistance and passivation quality. Control samples for thermal oxide grown under atmospheric pressure at 600 °C for 5 min were measured successfully, suggesting a thickness of 1–2 nm while providing excellent fit to SiO_2 models. It is possible that exposure of the ultra-thin tunnel oxide to atmospheric conditions causes additional native oxide growth which interferes with obtaining a reliable measurement. A precise thickness of the insitu tunnel oxide will likely have to be obtained from the completed oxide-polysilicon layer using transmission electron microscopy of cross sections of the samples, which were not performed for this investigation. The interfacial oxides are therefore referred to only by the process temperature and time.

The phosphorus doping sequence was performed in a separate diffusion furnace using $POCl_3$ dopant source, where the deposition was performed at temperatures between 700 °C and 850 °C, followed by N_2 anneal at 850 °C or 900 °C for 30 min to drive in the dopants. The samples were then annealed in a forming gas ambient (FGA) consisting of 5% H_2 and 95% N_2 for 30 min at 400 °C prior to lifetime measurements. The lifetime measurements were undertaken with a Sinton Instrument WCT-120 lifetime tester and the surface recombination prefactor, J_0 is deduced using the method of Kane and Swanson [25], assuming the Auger model of Richter et al [26], intrinsic carrier concentration of 9.7×10^9 cm^{-3} [27], and effective intrinsic carrier concentration calculated using an injection dependent band-gap narrowing model [28]. The uncertainty of the J_0 measurement represents the 95% confidence interval of the fit to the inverse lifetime curve. The sheet resistance, R_{sheet} presented within this paper represents R_{sheet} for a single side of polysilicon passivated surface, derived by deducting the wafer bulk R_{sheet} from the total R_{sheet} as determined using the Sinton WCT-120 lifetime tester.

Contact resistivity samples were fabricated from the lifetime samples by evaporating Aluminum with 99.999% purity in the patterns used by Cox and Strack [29]. The samples were then annealed in FGA at 250 °C for 10 min to provide good ohmic contact. A modified TMAH etch solution doped with silicic acid was used to etch back polysilicon and c-Si while leaving the Al and Al masked regions intact [30]. The measured resistance on each sample was fitted to 3D numerical simulation to resolve the contact resistivity, ρ_c.

3. Results and discussions

3.1. Surface passivation

The key characteristic of a passivated contact is the quality of its surface passivation, quantified here by the resulting J_0, which encompasses recombination within the polysilicon layer, the oxide interface, as well as the diffused region in the base Si wafer. The process of doped Poly-Ox deposition is relatively complex, involving three distinct steps: the tunnel oxide growth; polysilicon deposition and; dopant diffusion. While the number of experimental parameters ranging from temperature, time, and gas flow ratios at each step surmounts to quite a significant number of possibilities, this paper focuses on the results from varying only two key parameters: the oxidation temperature, which governs the tunnel oxide thickness; and the phosphorus diffusion temperature, which controls the depth and surface concentration of the phosphorus diffusion.

The first set of results presents the correlation between oxidation and phosphorus diffusion temperature to the surface passivation. The results are presented in Fig. 1(a) and (b), which plots the J_0 and R_{sheet} versus the oxidation temperatures performed on 1 Ω cm and 100 Ω cm n-type wafers. The oxide is grown within a low pressure condition of 600 mTorr for 10 min, and annealing was performed at 900 °C for 30 min in a nitrogen ambient. All other deposition and diffusion conditions are held constant for all samples as specified in Section 2.

Fig. 1(c) and (d) illustrates the deduction of the J_0 values for the best measured data on each phosphorus diffusion for the 1 Ω cm and 100 Ω cm n-type wafers. Some injection dependence is observed in these figures, as well as in the lifetime curve in Fig. 3(b). At this stage, the source of this injection dependence can not be fully ascertained to either bulk recombination or otherwise. However, irrespective of the cause, such electrical characteristics warrants the need to clearly define that all reported J_0 values in this work is extracted at an excess carrier density, Δn of 3×10^{15} cm^{-3}, representing the maximum power point of a highly efficient silicon solar cell.

The results within the explored set of parameters provide three key observations. Firstly, that a higher oxidation temperature provide lower J_0. Secondly, that this is strongly correlated to the measured R_{sheet}, where a low J_0 typically corresponds with a high R_{sheet}. Finally, it is important to note that the condition for excellent passivation is rather robust, where J_0 values below 3 fA cm^{-2} for 1 Ω cm wafers (and < 5 fA cm^{-2} for 100 Ω cm wafers) was achieved for a large range of conditions with oxidation between 700–800 °C and for all trialled phosphorus diffusion temperatures. It is notable that the lowest J_0 was measured at 0.3 ± 0.8 fA cm^{-2} measured on a 1 Ω cm wafer.

To further understand the complex relationship between J_0, R_{sheet}, oxidation temperature and phosphorus diffusion temperature, we measure and compare the doping profiles as measured via ECV, which provides a measure of the electrically active doping concentration. The