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Passivation property of ultrathin SiO_x:H / a-Si:H stack layers for solar cell applications

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ABSTRACT

A stacked layer of ultrathin hydrogenated silicon oxide (SiO_x:H) and hydrogenated amorphous silicon (a-Si:H) has been developed to passivate the crystalline silicon (c-Si) surface (see graphical abstract). Silicon oxide has the advantage of excellent optical and passivation properties. The SiO_x:H layer is deposited on the c-Si surface by atomic layer deposition (ALD), with its thickness precisely controlled below 2 nm. The a-Si:H layer is deposited on the SiO_x:H layer by plasma-enhanced chemical vapor deposition (PECVD) with a specific doping property, i.e. intrinsic, n- or p-type. The samples are then annealed in the range of 100 °C to 950 °C to study the fundamental passivation properties. We find that a combination of an ultrathin SiO_x:H and (p) a-Si:H layers shows a favorable passivation compared to a neat (p) a-Si:H layer. The effective minority carrier lifetime, measured by quasi-steady-state photoconductance (QSSPC), is ~ 0.5 ms after low temperature annealing at 300 °C. The passivation property is discussed in terms of hydrogen concentration, bond configurations, stoichiometry x of SiO_x:H, and material microstructure, characterized by Fourier transform infra-red (FTIR) and Raman spectroscopy. It is suggested that a reorganization of both the SiO_x:H, and the (p) a-Si:H layers, associated with hydrogen diffusion, plays an important role in improving the passivation.

1. Introduction

Silicon heterojunction (SHJ) is one of the most promising structures for solar cell devices regarding its conversion efficiency and the thermal budget necessary for its fabrication. In this type of solar cell, the junction is often formed by hydrogenated amorphous silicon (a-Si:H) doped and un-doped stack layers over the crystalline silicon (c-Si), where the intrinsic (undoped) a-Si:H layer provides an excellent passivation of the c-Si surface as well as charge carrier transport to the circuit contacts. Recently, a power conversion efficiency (PCE) record of 26.7% was obtained by Kaneka Corporation [1], previously held for two years by Panasonic at 25.6% [2]. Those efficiencies approach the efficiency limit estimated about 29.4% for a monocrystalline silicon cell with an optimized wafer thickness of ~ 110 μm, which still leaves room for further improvement of existing technologies [3,4]. Indeed, a high open circuit voltage of 750 mV is demonstrated using thin wafers of 98 μm [5], and even 753 mV reported with 50 μm-thick wafers [6], which makes optical current losses even more critical [7].

Considering the solar cell structures that successfully reached a PCE over 25% (Kaneka [1,8], Fraunhofer TOPCon [9], Panasonic HIT [2], SunPower IBC [10], UNSW PERL [11]), one can underline that the tunnel oxide passivated contacts (TOPCon) structure from Fraunhofer institute kept the design and fabrication process rather simple [9], with a recent improvement in terms of PCE to 25.8% on n-type silicon wafers in 2017. The TOPCon structure has an ultrathin oxide (SiO_x) passivation layer of ~ 1.4 nm over the c-Si wafer [12]. The thickness of this layer should be well controlled and below 2 nm to allow the tunneling of photogenerated carriers through it [12] (see the graphical abstract). Such an ultrathin oxide layer is usually formed by wet-chemical [12] or by UV-O_3 treatment [13], however the high temperature annealing at ~ 850 °C is required to achieve the high quality passivation and carrier transport. Thus, the development of low-temperature processes/annealing of this type of solar cells is beneficial in terms of the thermal budget, related to the production cost.

In order to reach such high-PCE solar cells, the surface passivation of c-Si wafer is one of the key points. The surface passivation, i.e. reducing the surface recombination velocity (SRV), is evaluated with the minority carrier lifetime (MCLT). The MCLT limit has been theoretically and experimentally demonstrated as a function of the dopant concentration in c-Si wafers [14]. Considering an n-type doped silicon wafer with a resistivity of 3 ± 2 Ωcm at room temperature, the effective MCLT is estimated to be ~ 8 ms for 1 Ωcm wafers and up to ~ 35 ms for 5 Ωcm wafers [14]. The thickness of passivation layers is also crucial, and creates a large difference in the effective MCLT. Thick

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passivation layers (~ 20 nm or more) are usually used for the evaluation of the effective MCLT [15], however actual solar cell devices must have thin passivation layers 10 nm or below for an a-Si:H layer in the SHJ and 2 nm or below for a SiO_x layer in the TOPCon. Here, one can note that the passivation and carrier transport are often competitive, and therefore these thicknesses should be optimized to achieve high-efficiency solar cells. An ideal passivation layer must fulfill the following specifications: (i) transparent to the solar spectrum, (ii) an excellent termination (passivation) of the Si dangling bonds over the c-Si wafer surface, and (iii) permeable to specific carriers to be collected at the contacts. The thermally grown silicon oxide mostly satisfy these requirements with an excellent passivation, with a MCLT about 29 ms for 90 Ωcm n-type silicon wafers 265 μm-thick [16], close to the theoretical limit. However, the carrier transport (extraction) in this thermally grown silicon oxide is highly limited due to the thickness and the transport barrier offset.

In this paper, we study the passivation property of ultrathin silicon oxide / a-Si:H stack layers for solar cell applications. The ultrathin silicon oxide is prepared by atomic layer deposition (ALD), which allows us to precisely control its thickness. Furthermore, hydrogen (H) atoms are intentionally incorporated into the films through this technique in order to enhance the passivation property. The a-Si:H layer is prepared by a conventional technique of plasma-enhanced chemical vapor deposition (PECVD), operated at 13.56 MHz capacitively coupled discharge. The samples are thus prepared using a *low temperature process* of < 300 °C, and then annealed from 100 °C to 950 °C at 50–100 °C steps for 30 min. At each annealing step, the effective MCLT is measured to evaluate the passivation property, and the material microstructure is characterized by using Fourier transform infra-red (FTIR) and Raman spectroscopy. The favorable passivation property of ultrathin SiO_x:H and (p) a-Si:H layers is obtained by *low temperature annealing* at 300 °C. The passivation property is discussed in terms of the material microstructure, including Si-H_x and Si-O_x bond configuration and a degree of the structural ordering.

2. Experimental

2.1. Silicon wafer cleaning

In this study, floating zone (FZ) silicon wafers (n-type doped, 1–5 Ωcm, 280 μm-thick, oriented ⟨100⟩, and polished double sides) were used. We started experiments with wafer cleaning, based on our standard cleaning process [17]. The wafer cleaning is a key process to ensure low impurity concentration over the wafer surface that reduces the defect states at the interface between the c-Si surface and the passivation layer. The cleaning process consists of (i) native oxide removal and chemical oxide growth by a self-heated piranha solution at 75 °C for 15 min (H_2SO_4:H_2O_2 ratio 4:1), (ii) an oxide etching for 2 min (HF:HCl:H_2O ratio 1:1:20), followed by (iii) an oxide growth for 15 min (HCl:H_2O_2:H_2O ratio 1:1:5), then (iv) oxide removal and surface termination by H atoms, using a diluted HF solution for 30 s (HF:H_2O ratio 1:20) as the last step. We also performed another wafer cleaning using a single step of HF + NH_4F 1 min etching. Compared with this clearing process, the above mentioned 4-step process shows a better passivation property in terms of the homogeneity and reproducibility.

The cleaned wafers were transferred into a vacuum box between each process in order to reduce the oxidation and contamination. The H-terminated surface of silicon wafers is stable for ~ 30 min in ambient air [18,19], which makes this cleaning process relevant for the study of ultrathin SiO_x:H properties.

2.2. Sample structures

The cleaned c-Si wafers were passivated by a stacked layer of silicon oxide and a-Si:H for both front and back sides, giving a symmetric structure. Several different structures were fabricated with a combination of silicon oxides as a interfacial layer and a-Si:H as an over-coating upper layer. The silicon oxide layers were controlled with or without the incorporation of H atoms (SiO_x:H or SiO_x) by choosing the ALD condition, as described in the next Section. Doped n- or p-type as well as non-doped intrinsic (i) a-Si:H were prepared for the a-Si:H upper layer by controlling the dopants. Table 1 summarizes the structures fabricated in this study.

Table 1
Sample structures prepared in this study. A stacked layer of silicon oxide and a-Si:H was employed. For references, a neat layer of silicon oxide and a-Si:H was prepared. Both the c-Si front and rear surfaces were passivated symmetrically with these layers.

a-Si:H doping type	with SiO_x layer	with SiO_x:H layer
(i) a-Si:H / c-Si / (i) a-Si:H	(i) a-Si:H / SiO_x / c-Si / SiO_x / (i) a-Si:H	SiO_x:H / c-Si / SiO_x:H (i) a-Si:H / SiO_x:H / c-Si / SiO_x:H / (i) a-Si:H
(n) a-Si:H / c-Si / (n) a-Si:H	(n) a-Si:H / SiO_x / c-Si / SiO_x / (n) a-Si:H	(n) a-Si:H / SiO_x:H / c-Si / SiO_x:H / (n) a-Si:H
(p) a-Si:H / c-Si / (p) a-Si:H	(p) a-Si:H / SiO_x / c-Si / SiO_x / (p) a-Si:H	(p) a-Si:H / SiO_x:H / c-Si / SiO_x:H / (p) a-Si:H

2.3. Depositions of silicon oxide and a-Si:H, and post-deposition annealing

The ultrathin silicon oxide layers of SiO_x or SiO_x:H were deposited using ALD (Oxford Instruments FlexAL® system). The deposition temperature was set to 300 °C throughout the ALD process. The precursor of tris(dimethylamino)silane (3DMAS) was used as a silicon source. An oxygen (O_2) plasma was used as an oxygen source, generated by an inductively coupled plasma (ICP) with 13.56 MHz RF at O_2 pressure of 15 mTorr for 3 s. The incorporation of hydrogen in the SiO_x:H layer was carried out by a H_2 plasma using ICP-RF at a H_2 pressure of 38 mTorr for 20 s. For both O_2 and H_2 plasma processing steps, the RF power was set to 250 W forward and 0 W reverse in auto-match mode without any intentional bias on the stage where samples were located. Thus, the stage was floating, i.e., not electrically grounded to the chamber. This floating condition yields a low ion energy with a relatively narrow energy distribution [20,21], which is expected to reduce the surface damage during plasma processing. The processing gas was purged for 2–5 s at each plasma step to evacuate the residuals. Besides, the processing gas was pumped out for 60 s before and after H_2 plasma step to avoid gas mixture of O_2 and H_2. The thickness of silicon oxide during the ALD was monitored by spectroscopic ellipsometry (SE) in situ using a Cauchy model. We controlled the thickness by adjusting the number of ALD cycles, $0.8 - 1.2 \pm 0.1$ nm for SiO_x layer and $0.2 - 2.4 \pm 0.1$ nm for SiO_x:H layer.

The c-Si wafers were then transferred into PECVD system for the deposition of a-Si: H. The non-doped (i) a-Si:H layer was deposited at 180 °C using pure silane (SiH_4) gas, the n-type a-Si:H was deposited at 200 °C with a mixture of SiH_4, H_2 and PH_3, and the p-type a-Si:H was deposited at 150 °C with a mixture of SiH_4, H_2, and B_2H_6. The thicknesses of a-Si:H layers were 20 ± 1 nm for both (i) and (n) a-Si:H layers and 23 ± 1 nm for (p) a-Si: H, determined from SE assuming a Tauc-Lorentz model.

After the fabrication in the above mentioned manner, the samples were annealed in a vacuum furnace. The annealing temperature, *T*, was increased from 100 °C to 950 °C with an interval of 50–100 °C and the annealing period was fixed to 30 min.

2.4. Characterization of passivation and material structure

At each annealing step, the passivation and material microstructure were characterized at room temperature in ambient air using conventional methods: quasi-steady-state photoconductance (QSSPC) [22], FTIR and Raman spectroscopy. The passivation property was evaluated