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Improved mechanical strength and reflectance of diamond wire sawn multi-crystalline silicon wafers by inductively coupled plasma (ICP) etching

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ABSTRACT

In this work the standard wet chemical and plasma texturing processes for multi wire slurry abrasive sawn multi-crystalline silicon were applied to fixed diamond wire sawn (DW) multi-crystalline silicon. The plasma etch produced an effective anti-reflective layer without any changes to the process parameters. The achieved texture features a reflectance well below 5% in the visible range. Furthermore the mechanical strength of the wafers was investigated. 4-point bending tests revealed that anisotropic strength behavior is still present for the plasma textured wafer. In addition to their excellent optical properties, the plasma textured wafers show increase of 123% in characteristic fracture stress related to the as-cut batch for the critical loading with the saw marks parallel to the rollers. This can lead to a significantly reduced breakage rates during solar cell production. It is shown, that the characteristic fracture stress of the multi-crystalline plasma textured batch is equal to the strength of mono-crystalline industrial wet etched fixed diamond wire sawn wafer.

1. Introduction

In order to produce solar cells with mono-crystalline silicon wafers the fixed diamond wire sawing (DW) has become the predominant technology with predicted increasing market share of about 95% in 2018 [1]. For multi-crystalline silicon (mc-Si) the slurry abrasive sawing (SL) technique is still the predominant technology. The market share for mc-Si SL is predicted to decrease but is still very high with about 65% in 2017 [1]. One reason is the significant process improvements of SL with the change from straight to structured wires [2]. Other reasons are higher wire consumptions for DW compared to mono-Si and insufficient performance with standard wet chemical etching processes on DW mc-Si wafers. The two sawing technologies SL and DW producing very different wafer surfaces because of the differences in the silicon removal processes which leads to different roughness and structure of surface cracks. The directed median cracks for the DW wafers lead to a strong anisotropic strength behavior with a lower strength compared to the SL wafers for the weakest loading direction [3]. Furthermore, the surface structure of the DW mc-Si wafers is responsible for the etching problems [4], since a specific surface near defect structure is essential for the etching process. In order to etch DW wafers wet-chemically, extensive changes to the process-pipeline are needed, like an additional polishing step for single crystalline wafers [5] or using a metal catalyst [6] or additives [7] or a mechanical pre-treatment [8] for multi-crystalline wafers.

In contrast, plasma processes proved to be independent on crystallographic orientation and surface roughness [9]. One popular method of creating an effective anti-reflective silicon texture is the "Black Silicon Method", proposed by Jansen et al. [10]. The light trapping in the resulting silicon structures is similar as in moth-eyes, which act as a zero or first order effective medium due to a continuous refractive index transition [11,12]. Often, black silicon is achieved by using an additional self-bias to accelerate ions to the wafer surface. However, the resulting surface damage has a negative influence on effective carrier lifetimes and therefore also on the final conversion efficiency. Thus, a pure inductively coupled plasma (ICP) process was developed [13], which was optimized for industrial mass production, without additional self-bias. Also, a saw defect removal (SDR) step was included by means of a pure SF6 inductively coupled plasma. The reduced ion bombardment leads to reduced surface damages and increased effective carrier lifetimes, compared to classical capacitive coupled plasma (CCP) processes, which apply typically a self-bias [14]. Furthermore this plasma texturing step proved to be highly flexible as the same ICP process can be used to texture slurry sawn, diamond wire sawn, kerfless-separated, single- and multi-crystalline wafers without any changes. This flexibility may popularize both DW techniques and plasma processing in PV

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industry. In this work, the optical and mechanical properties of plasma textured diamond wire sawn multi-crystalline silicon wafers are analyzed.

2. Material and methods

For the investigations 300 DW (electroplated) 15.6 × 15.6 cm^2 full square multi-crystalline Si wafers with a medium thickness of 200 µm were processed, sorted into three different batches (Batch 1: as-cut, Batch 2: wet chemical-etch, Batch 3: plasma-etch). Each batch consists of 100 Wafers, sorted in a way that each batch represents the overall multi-crystalline crystal structure in the Si brick. Batch 1 (as-cut) is used as reference for strength and reflectance measurements. Batch 2 was etched by a $CH_3COOH/HNO_3/HF$-mixture. We textured Batch 3 with a recently developed maskless ICP texturing process. After wet and plasma texturing, the global reflectance and fracture strength of the wafers were measured. In the following, each experimental step is explained in more detail.

2.1. Plasma texturing

The used plasma process was thoroughly investigated and discussed for slurry sawn Si substrate materials in [13] and is optimized for industrial mass production. This plasma process is suited to process c-Si, mc-Si, SL and DW wafers without any changes. A short overview of the process parameters is given in this paragraph.

For plasma texturing an Oxford Plasmalab 100 ICP 65 system is used. The alternating field of the inductively coupled plasma (ICP) source is operating at 13.56 MHz. For all plasma steps, an ICP power of 600 W was set. By using only an ICP source without additional self-bias, minimal surface damage and better charge carrier lifetimes can be expected [14]. The wafers were mechanically clamped to the lower electrode by a graphite clamp that is holding the wafer at two opposite sides. The lower electrode is cooled by a chiller and held to 5 °C during all plasma processes.

At first, a saw damage removal (SDR) by pure SF_6 plasma, at 50 µbar pressure was carried out. The average etch rate of this process, determined by measuring the weight difference of wafers before and after etching, is 1.1 $\mu m\,min^{-1}$. However, the process is inhomogeneous, having far lower etch rates at the wafer margins, due to the size of the ICP coil (65 mm diameter). Thus, the SDR was performed for 12 min, to ensure a minimum etch depth of 5 µm at the wafer margins. After the SDR, a 4 min pure Oxygen plasma step (50 µbar) was done to initialize the wafer surface to allow a homogenous maskless texturing process. Then, an ICP texturing step with an SF_6/O_2 gas mixture at a gas ratio of 2:1 was carried out for 20 min at 17 µbar.

This plasma step produces parabolic pits with a diameter of about 500 nm and a depth of roughly 1 µm. A SEM image of such a structure is shown in Fig. 1. Half of the full sized wafers were clamped parallel to the saw marks, the rest perpendicular to the saw marks to allow for directional bending tests later on. Calculated from the average thickness of the plasma textured batch compared to the as-cut batch 15 µm of silicon was removed by the plasma process on one side.

2.2. Wet chemical texturing

For wet chemical etching a non-optimized lab scale process was used. The samples were etched in a 3.5 L bath at room temperature. The etching solution contained 0.89 L of CH3COOH (98% VLSI), 2.25 L of HNO3 (69% VLSI) and 0.53 L of HF (48% VLSI). The exothermic reaction was leading to a temperature increase up to 60 °C. The removal rate were controlled over time and measured after the texturization by differential weighing. After etching the wafers were cleaned with high-purity water and dried at room temperature. Calculated from the average thickness of the wet chemical etched batch compared to the as-cut batch 12 µm of silicon was removed by the wet chemical process on both sides together.

2.3. Optical measurements

The optical measurements were obtained in an integrating sphere from Perkin Elmer, equipped with a Lambda 1050 UV/VIS/NIR spectroscope. The hemispherical reflectance of 5 samples for each batch, wet-chemical, plasma textured, and as-cut were measured, respectively. For each wafer, the reflectance was measured in the center as well as at the margin (face diagonal) of the wafer.

2.4. Fracture tests

For analyzing the mechanical strength of wafers fracture tests the 4-point bending setup is used following [15], because it loads a large area homogenously by uniaxial bending moments including the surface and edge defects of the wafer. The load occurs as homogeneous tensile stress on the bottom surface of the wafer in the test. The 4-point bending configurations in this work had an outer span (outer rollers) of 110 mm and inner load span (inner rollers) of 55 mm. The rollers are made of steel with a diameter of 10 mm. For better contact behavior and reduced friction PTFE foils were put between the rollers and the wafers. The wafers are loaded in two different configurations with the saw marks parallel and across to the loading rollers.

In each experimental batch 50 wafers were tested. All tests were performed on a universal testing machine ZWICK 005, using a load cell of 500 N. The deflection of the sample was measured by the machine position. The load speed was defined to be 0.05 mm/s. During testing the force and deflection was recorded for each sample, beginning after reaching an initial force of 0.5 N and ending at the fracture of the wafer.

Afterwards, a Finite Element model was used to calculate the fracture stresses in the 4-point bending experiment. Then, the fracture stresses σ_i were statistically evaluated using a two parameter Weibull distribution [16,17]

$$P = 1 - \left[\exp\left(-\frac{\sigma_i}{\sigma_\theta}\right)^m\right]$$

where σ_Θ is the characteristic fracture stress at which 63.2% of all

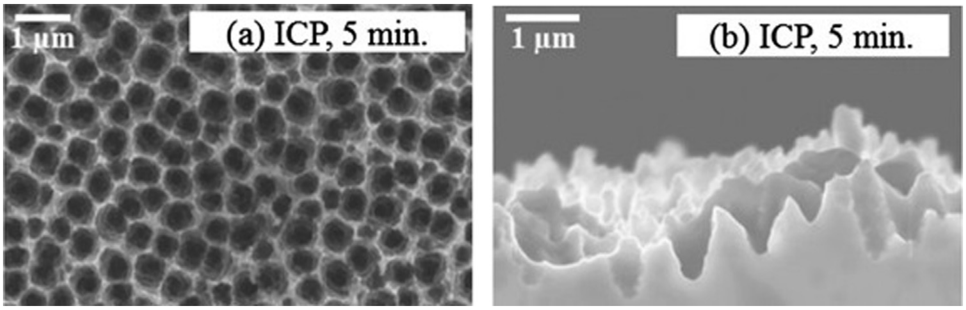

Fig. 1. SEM images of an ICP texture on single crystalline silicon from top view (a) and across section (b) after 5 min ICP etching [13].