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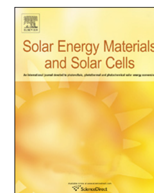

Temperature-dependent contact resistance of carrier selective Poly-Si on oxide junctions

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ABSTRACT

Carrier selective junctions using a poly-silicon/ silicon oxide stack on crystalline silicon feature low recombination currents J_0 whilst allowing for low contact resistivity ρ_C. We describe the limiting current transport mechanism as a combination of homogeneous tunneling through the interfacial silicon oxide layer and transport through pinholes where the interfacial silicon oxide layer is locally disrupted. We present an experimental method and its theoretical basis to discriminate between homogenous tunneling and local pinhole transport mechanisms on $n+/n$ or $p+/p$ junctions by measuring the temperature-dependent contact resistance. Theory predicts opposing trends for the temperature dependencies of tunneling and pinhole transport. This allows identifying the dominant transport path. For the contact resistance of two differently prepared poly-Si/ silicon oxide/ c-Si junctions we either find clear pinhole-type or clear tunneling-type temperature dependence. Pinhole transport contributes more than 94% to the total current for the sample with a 2.1 nm-thick interfacial silicon oxide that we anneal at a temperature of 1050 °C to achieve highest selectivity. In contrast pinhole transport contributes less than 35 % to the total current for the sample with a 1.7 nm-thick silicon oxide that we annealed at only 700 °C in order to avoid pinholes.

1. Introduction

One keystone in achieving a high conversion efficiency with solar cells is to form carrier selective contacts to the light absorbing material that allow majority charge carriers to be collected at the contact without hindrance but impede the recombination of minority charge carriers. The selectivity, given as the ratio of the resistance of minority and majority charge carriers on their way to the contact [1] can be expressed as

$$S_{10} = \log_{10}\left(\frac{k_B T}{q \cdot J_0 \cdot \rho_C}\right) \tag{1}$$

where ρ_C is the contact resistance and J_0 is the dark saturation current density. The maximum efficiency that can be achieved by an otherwise ideal cell increases linearly with S_{10} and saturates for $S_{10} > 15$ to the maximum efficiency of Si solar cells [1]. Highest selectivities of $S_{10} = 16.2$ were realized on samples with *p*- and *n*-type poly-Si on oxide (POLO) junctions [2] and recently led to an interdigitated back contact solar cell with POLO junctions for both polarities with an independently confirmed energy conversion efficiency of 26.1% for a *p*-type Si wafer [3].

Carrier selective junctions with a stack of poly-Si/SiO_x/Si were modelled with tunneling transport [4] and with pinhole transport [5,6]. Both models explained the measured contact resistances and passivation qualities of the respective samples, even if the tunneling model has difficulties explaining the electrical properties of electron- and hole collecting poly-Si/SiO_x/Si junctions with consistent parameters as pointed out by Peibst et al. [5]. The existence of pinholes was proven for certain samples by structural and electrical analysis after annealing at temperatures as low as 750 °C [7–10]. For other samples strong evidence for tunneling was given [11]. The dominant transport mechanism depends on the type of sample and the preparation conditions. It is possible that technologically important cases show both mechanisms simultaneously as is schematically illustrated in Fig. 1. The interfacial oxide (yellow) is broken up locally to allow pinhole currents from the wafer into the poly-Si layer and allows tunneling currents where the interfacial silicon oxide is intact. During the high temperature anneal dopants can diffuse from the poly-Si layer through the oxide into the c-Si, forming a region with increased dopant density below the oxide, schematically shown as a fading red area in Fig. 1. The dimension of this in-diffused region depends on the type of sample and the annealing conditions.

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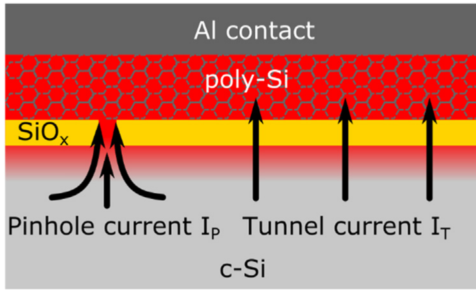

Fig. 1. Sketch of the pinhole and tunneling transport as parallel conduction paths in a carrier selective POLO junction.

We consider the global current I_G through the junction to be a sum of the current through pinholes (I_P) and through a tunneling barrier (I_T) at all the sites where the oxide is intact:

$$I_G = I_P + I_T \quad (2)$$

This work develops an experimental and theoretical framework to extract the contribution of each current type to the global current through a $n+/n$ or $p+/p$ junction from temperature-dependent contact resistance measurements. We thereby quantify the relative significance of both mechanisms in a single sample.

2. Theory

2.1. Pinhole contact resistance

Transport through pinholes is described by means of the semi-classical drift-diffusion model similar to point contacts for solar cells [12–14]. The spreading resistance

$$R_{Spread}(T) = \frac{\rho_B(T)}{2\pi r_P}\cdot\arctan\left(\frac{2W}{r_P}\right) \quad (3)$$

between a circular disc-shaped contact and a planar base contact was calculated in Ref. [12]. In the case of a POLO junction, we consider the resistance of a pinhole with radius r_P to be that between the poly-Si/ c-Si interface in the pinhole and a full area contact at distance W from the pinhole. Here, ρ_B is an average specific resistivity in the diffused area below the pinhole. The spreading resistance R_{Spread} of a single pinhole generally depends on the distance W. However we find that R_{Spread} saturates with increasing W as illustrated in Fig. 2. The characteristic distance on which this saturation occurs, only depends on the pinhole radius r_P and has a maximum value of W = 30 nm for reported pinhole radii in the range of 2.5–19 nm [8]. This means that the value of ρ_B in Eq. (3) must be understood as a weighted average of the specific resistance in a region of at maximum 30 nm below the pinhole. Insertion of the reported pinhole radii into Eq. (3) yields spreading resistances of 10 kΩ to 2 MΩ for a single pinhole as depicted in Fig. 2, assuming a specific resistance ρ_B of 70 mΩ cm^2. This value of ρ_B corresponds to a donor concentration of $N_{Dop} = 1.4\times10^{17}\text{cm}^{-3}$ as found for the pinhole sample presented below.

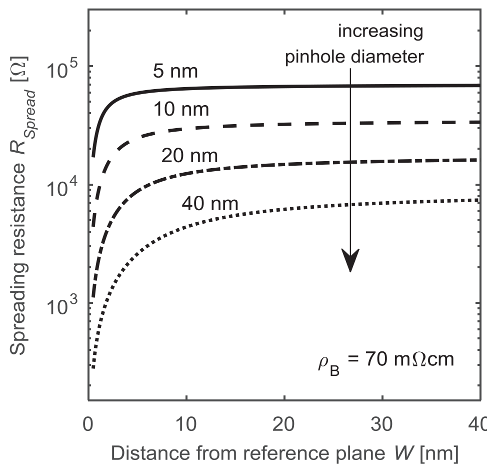

Fig. 2. Saturation of the spreading resistance with increasing distance from the pinhole site. The specific resistance below the pinhole ρ_B is set to a reference value of 70 mΩ cm which reflects our pinhole sample.

The total resistance of a field of pinholes with an areal density N_P is [5]

$$\rho_{C,P}(T) = \frac{R_{Spread}(T)}{N_P}. \quad (4)$$

The only temperature dependent factor in Eq. (3) is the bulk resistivity ρ_B. Its absolute value and temperature dependence depends on the dopant density N_{Dop} and is well parameterized [15–17]. In the doping and temperature range considered here ρ_B increases with increasing temperature. The pinhole density N_P is a constant for each sample and can range over many orders of magnitude depending on the sample preparation [7].

2.2. Tunneling contact resistance

Current-voltage characteristics of semiconductor insulator metal (MIS) contacts containing a thin insulator for tunneling were studied already in the 1970s [18–21]. Following [11] we treat the highly doped and degenerate poly-Si layer as a metal-like material, enabling the application of Card and Rhoderick's well established theory of an MIS tunneling junction [19]. Four types of currents can play a role in this theory: direct band to band tunneling and tunneling via trap states for majority and minority charge carriers, respectively. We ignore minority currents due to the small minority charge carrier densities expected in our samples for measurements in the dark and under small bias voltages [22]. Note that in the case of $p+$-type poly-Si/ n-type c-Si or $n+$-type poly-Si/ p-type -c-Si POLO junctions, minority currents cannot be ignored. However we do not consider such junctions here. Ignoring minority currents leaves us with direct tunneling and trap-assisted tunneling of the respective majority carriers. We will also disregard trap-assisted tunneling because this would require the knowledge of additional parameters that we do not have access to and discuss the case of valence band tunneling only. For conduction band tunneling the same expressions apply with the according parameters. The net current of direct tunneling from the poly Si into the wafer is [19,21,23]

$$J_T(V) = A^*T^2\mathrm{P_T}\exp\left(-\frac{\Delta E_S}{k_BT}\right)\left[\exp\left(\frac{qV}{n\cdot k_BT}\right)-1\right], \quad (5)$$

where $A^* = 4\pi qm^*k_B^2/h^3$ is the effective Richardson constant and

$$P_T = \exp\left(-d_{ox}\sqrt{\frac{8m_T}{\hbar^2}E_B}\right) \quad (6)$$

is the tunneling probability for a symmetric tunneling junction with the hole tunnel mass m_T, the effective mass m^* of the valence band and an ideality factor n that specifies the change of the surface potential at the oxide/ c-Si interface as a result of the applied voltage V [19]. The tunneling parameters that are shown in the schematic band diagram in Fig. 3 are the barrier height E_B of the tunneling barrier, the oxide thickness d_{ox} and the difference ΔE_S between the valence band and the Fermi-level at the oxide/ c-Si interface at zero bias. Eq. (5) was derived using Boltzmann statistics on the wafer side of the barrier. This approximation might not be fulfilled in a poly-Si/c-Si junction with a charge carrier density N_{Dop} below the oxide so high that Fermi statistics have to be applied.

The corresponding contact resistance at zero voltage is

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