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Effect of silicon oxide thickness on polysilicon based passivated contacts for high-efficiency crystalline silicon solar cells

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ABSTRACT

In this study, we have investigated the effect of SiO_x thickness (1–3 nm) on the performance of polycrystalline (poly) Si/SiO_x/monocrystalline Si (*c*-Si) passivated contacts. Our results show that for both *n*- and *p*-type contacts, there is an optimum SiO_x thickness of 1.4–1.6 nm for obtaining the highest implied open-circuit voltage (*i*-V_{oc}) values of ~739 and ~700 mV, respectively. For contacts with SiO_x thicker than 1.6 nm, the *i*-V_{oc} drops due to reduced field-effect passivation. We attribute this to the fact that a thicker SiO_x layer hinders the diffusion of both *n*- and *p*-type dopants into the *c*-Si wafer resulting in a junction that is very close to the *c*-Si/SiO_x interface, which increases carrier recombination most likely due to the presence of defects at this interface. The resistivity measured through the metal/poly-Si/SiO_x/*c*-Si stack is independent of SiO_x thickness up to 1.6 nm, and increases exponentially by several orders of magnitude with further increase in SiO_x thickness due to inefficient tunneling transport. Finally, the extent of metallization-induced degradation of the poly-Si/SiO_x/*c*-Si contacts is worst for the thinnest SiO_x investigated (~1 nm), and interestingly it is not completely mitigated even for a ~3 nm thick SiO_x.

1. Introduction

Monocrystalline Si (*c*-Si) solar cells with passivated contacts based on the ultrathin SiO_x and doped polycrystalline Si (poly-Si) layers in a metal/poly-Si/SiO_x/*c*-Si structure can achieve efficiencies > 25% [1,2]. These contacts use a 1–2 nm thick tunneling SiO_x on *c*-Si, and doped poly-Si on SiO_x, to create a poly-Si/SiO_x/*c*-Si passivated contact structure [3–5]. The separation of the doped poly-Si layer from *c*-Si through SiO_x is critical as it provides a very low recombination interface to the wafer and prevents the epitaxial growth of the poly-Si layer during the required high temperature annealing of these contacts. The ultrathin ~1–2 nm SiO_x enables electrical transport via tunneling [6–8] and/or pinholes in the SiO_x layer [9–11], and is a very good surface passivation layer for *c*-Si due to the low *c*-Si/SiO_x interfacial defect densities [12,13]. Additional field-effect passivation is obtained due to the heavily doped poly-Si layer deposited on the tunneling SiO_x layer. A combination of these two passivation mechanisms leads to a very low emitter recombination current density, J_o [9,14,15]. The separation of the metal contacts from the *c*-Si absorber, via the use of the doped poly-Si/SiO_x stack helps reduce the metallization-induced carrier recombination, while enabling carrier separation and collection.

The high-temperature stability, excellent passivation, and manufacturing flexibility demonstrated by these contacts make them a suitable candidate for next-generation *c*-Si solar cell technologies. However, to incorporate them into industrial-scale manufacturing, it is important to understand their salient features while identifying the allowed processing windows for these contacts. Currently, in the literature, different techniques have been reported for the fabrication of the poly-Si/SiO_x/*c*-Si contacts. The SiO_x layer can be grown either via dry thermal oxidation [16], or by chemical oxidation with nitric acid [4,5] or UV/O_3 [17]. Even though these SiO_x films have different stoichiometry, surprisingly they show marginal effect on the final passivated contact performance [17]. The doped poly-Si film can be grown via either plasma-enhanced chemical vapor deposition (PECVD) [4,16] or low-pressure chemical vapor deposition [5]. Additionally, these poly-Si films can be doped in numerous ways such as during growth of amorphous Si (*a*-Si) [16], ion-implantation of intrinsic poly-Si [5], $POCl_3$ and BBr_3 thermal diffusion [18], or with suitable dopant pastes and inks [19]. The morphology of the doped Si layers can be either polycrystalline [16], microcrystalline [4], or an amorphous

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matrix embedded with Si nanocrystallites [20]. However, even with all these variabilities, the final contact performance is similar, with implied open-circuit voltage (i-V_{oc}) values being ~735–740 mV for phosphorous doped n-type and ~700–710 mV for boron doped p-type contacts [4,16]. The only common feature in these contacts is that the SiO_x layer is ~1.5 nm thick, and the contacts need to be annealed between 850 and 900 °C after a-Si deposition for obtaining the highest i-V_{oc} values. The loss of performance upon annealing above 900 °C has been attributed to significant SiO_x break-up, which results in localized loss of the chemical passivation provided by the SiO_x layer [21,22]. A different approach, the poly Si on oxide (POLO) [10,18] contacts reported by the Institute for Solar Energy Research in Hamelin (ISFH) have a very similar poly-Si/SiO_x stacked structure but with a thicker, ~2.2 nm, SiO_x. However, these contacts are processed at a much higher temperature of ~1000–1050 °C to achieve record high i-V_{oc} values of 748 and 729 mV for both the n- and p-type contacts, respectively [23]. For these POLO contacts, the higher temperature is quite crucial since it results in pinholes in SiO_x that provide direct conduction pathways between the poly-Si and underlying c-Si absorber resulting in very low through-contact resistivities [10,11,24].

In this study, we focus on understanding the role of the thickness of the thermally-grown SiO_x layer on the contact performance where the contact annealing temperature is limited to 850 °C. Under these conditions, we do not expect SiO_x breakup, which can significantly affect charge transport and surface passivation. We show that a SiO_x thickness within 1.4–1.6 nm leads to the highest i-V_{oc} values of ~739 and ~700 mV for n- and p-type contacts, respectively. We hypothesize that this SiO_x thickness range provides an optimum balance between the chemical passivation from the SiO_x layer and the field-effect passivation from the dopants, as both of these depend on the SiO_x thickness. We show that carrier transport through the contact reduces by several orders of magnitude when the SiO_x thickness is increased from 1.6 to 1.9 nm due to inefficient tunneling. Finally, we show that the extent of metallization-induced degradation of the poly-Si/SiO_x contacts is worst for the thinnest SiO_x investigated (~1 nm), and interestingly is not completely mitigated even for a ~3 nm thick SiO_x.

2. Experimental details

As-sawn, phosphorous-doped, n-type Czochralski (n-Cz) Si(100), 8 Ω-cm resistivity, ~190 µm thick wafers (Woongjin Co. Ltd., South Korea) were subjected to a KOH based etch for planarization and saw-damage removal. The wafers were then cleaned using standard wafer cleaning procedures of piranha, RCA-1 and RCA-2 [25,26], followed by a treatment with 1% aqueous HF to remove the SiO_x formed as a result of the RCA-2 cleaning process. A dry thermal SiO_x film was then grown on the wafers in a quartz tube furnace at nearly atmospheric pressure with a 6:1 N_2-to-O_2 gas flow ratio. The thermal SiO_x thickness was varied by changing the oxidation time between 0.5 and 30 min for temperatures between 700 and 800 °C. The SiO_x thickness at each oxidation condition was determined by spectroscopic ellipsometry on single-side-polished n-Cz Si(100), 1–100 Ω-cm resistivity wafers that were loaded into the furnace at the same time as the saw-damage removed wafers.

Doped a-Si:H was then deposited on both sides of the oxidized c-Si wafers using a SiH_4/H_2 capacitively-coupled, radio-frequency plasma powered at 13.56 MHz. The flow rates of SiH_4 and H_2 were 2 and 100 standard cm^3/min (sccm), respectively. Additionally, for boron or phosphorous doping, 1 sccm of B_2H_6 (2.6% in H_2) or PH_3 (3% in H_2) were introduced into the chamber. The c-Si wafer was placed on the grounded substrate holder at a temperature of 300–350 °C with an input power to the plasma source of 8 W to grow a ~20 nm thick a-Si:H layer. The resulting samples were then annealed at 850 °C for 30 min in a quartz tube furnace under N_2 atmosphere to convert a-Si:H to a poly-Si layer via solid-phase crystallization. A hydrogen-induced passivation step followed, which involved deposition of Al_2O_3 via atomic layer deposition using trimethylaluminium and H_2O as precursors at 200 °C followed by annealing in forming gas (1:9 H_2:N_2 mixture) at 400 °C for 20 min. Quasi-steady-state photoconductance decay measurements were performed using a Sinton lifetime instrument (WCT-120) to extract the i-V_{oc} values [27] for symmetric test structures on saw-damage removed wafers, similar to those shown in the inset of Fig. 1. Dopant depth profiles through the poly-Si layer into the c-Si wafer were measured on single-side-polished samples via secondary ion mass spectrometry (SIMS) using 1.5 keV ion bombardment energy from an oxygen source.

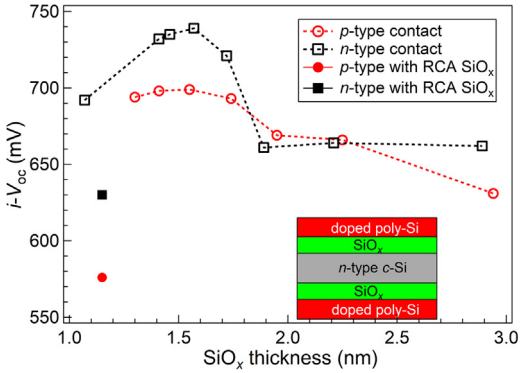

Fig. 1. Effect of thermally grown SiO_x thickness on the i-V_{oc} of symmetric n- (□) and p-type (○) passivated contact test structures shown in the inset. The i-V_{oc} for n- (■) and p-type (●) passivated contacts with ~1.15 nm thick RCA SiO_x is shown for comparison. The dashed lines are a guide to the eye.

On the symmetric poly-Si/SiO_x/c-Si/SiO_x/poly-Si structures on the saw-damage removed wafers, using suitable shadow masks, ~1 µm thick Al was deposited via electron beam (e-beam) evaporation in a tool with a base pressure of $\sim 10^{-7}$ Torr. Aluminum was deposited either as a $3 \times 2\,cm^2$ pad to determine metal-induced degradation, or as rectangular or circular pads that were much smaller in size, for resistivity measurements. Post-metallization, the n-type contact samples were annealed at 400 °C in forming gas for 5 min, since previous experiments [16] show that it results in lower metallization-induced degradation of the contact. However, the p-type contact did not require a post-metallization anneal. Metallization-induced degradation was determined using photoluminescence (PL) imaging, which measures the intensity from radiative carrier recombination in the sample under steady-state conditions at a fixed illumination intensity and wavelength [28]. The poly-Si layer sheet resistivity, and the Al to poly-Si contact resistivity was determined using the smaller rectangular Al pads with varying spacing using the transmission line method (TLM) [29]. The structure with the TLM pattern was then subjected to reactive ion etching using SF_6 with the Al pads on the front as etching masks. After etching, the poly-Si and SiO_x layers were completely removed in the unmasked regions along with a few microns of the underlying c-Si. The opposite unmetallized side of the c-Si wafer was also etched to completely remove the poly-Si and SiO_x layers. The resulting structures were utilized to determine the through-contact resistivity for the n^+-n high-low junction by TLM analysis, and the diode resistivity at 0.59 V of the p^+-n diode from its current-voltage (J-V) curve.

3. Results and discussion

3.1. Effect of SiO_x thickness on c-Si surface passivation

Fig. 1 shows the effect of SiO_x thickness on the i-V_{oc} of symmetric n- and p-type passivated contact test structures shown in the inset. Contacts with thermally grown SiO_x show an i-V_{oc} that is at least 50 mV higher than the i-V_{oc} obtained for the RCA SiO_x with a very similar thickness, implying that the SiO_x growth method affects c-Si surface passivation. Also, there is a clear trend in Fig. 1, which shows that for