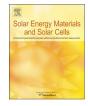
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Simple and versatile UV-ozone oxide for silicon solar cell applications

Sara Bakhshi^{a,b}, Ngwe Zin^{a,b,*}, Haider Ali^c, Marshall Wilson^e, Debashis Chanda^{b,d}, Kristopher O. Davis^c, Winston V. Schoenfeld^{a,b}

^a Florida Solar Energy Center, University of Central Florida, United States

^b College of Optics and Photonics, University of Central Florida, United States

^c Department of Materials Science and Engineering, University of Central Florida, United States

^d NanoScience Technology Center, University of Central Florida, United States

^e Semilab SDI LLC, United States

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ABSTRACT

Semiconductor surface clean is sometimes perceived as costly but long recognized as pivotal in determining the final semiconductor device performance and yield. In this contribution, we investigated the effectiveness of crystalline silicon surface cleaning by a simple UV-ozone process in comparison to the industry standard RCA clean for silicon photovoltaic applications. We present a unique method of processing the silicon surface effectively by UV-ozone cleaning. Despite being simple, UV-ozone cleaning results in a superior surface passivation quality that is comparable to high-quality RCA clean. When used as a stack dielectric—UV-ozone oxide overlaid by aluminum oxide—the thickness of UV-ozone oxide plays an important role in determining the passivation quality. Of all treatment times, 15 min of UV-ozone treatment results in an outstanding passivation quality, achieving the effective technique to extract values of electron/hole capture cross-section for the purpose of analyzing the interface passivation quality from already measured surface recombination parameters of saturation current density, interfacial trap density and total fixed charge, instead of measuring on the separately prepared metal-insulated-semiconductor (MIS) samples by the techniques: frequency-dependent parallel conductance or deep-level transient spectroscopy.

1. Background

Semiconductor surface cleaning is sometimes seen as a costly process as it consumes a significant amount of chemical resources and can require considerable waste disposal. However, it is accepted that an effective surface cleaning leads to improved device performance. Over the years, various types of crystalline silicon (c-Si) wafer cleaning sequences have been applied, based on the mixture of NH₄OH+H₂O₂, HCl+H₂O₂ and HF [1]; plasma etch [2], plasma treatment for smallgeometry devices [3], chlorine cleaning [4] and hydrogen peroxide as an oxidant in the chlorine cleaning [5] to remove photoresist, contaminants, particles, organic/inorganic impurities and native oxide on the silicon wafer surface. Wafer cleaning chemistry, based on hot alkaline and acidic hydrogen peroxide solution-called RCA (Radio Corporation of America) standard clean-has been the primary method of cleaning in the microelectronic industry [6]. RCA standard clean includes the mixture of NH₄OH/H₂O₂/H₂O, referred as SC-1, and HCl/ H₂O₂/H₂O, referred as SC-2. SC-1 removes the organic contaminants, while inorganic contaminants are removed by SC-2. Ultraclean

deionized water is used for intermediate and final rinses after SC-1 and SC-2, respectively [1]. However, the SC-1 was found to cause the surface damage, due to micro-roughness formed by NH₄OH [7]. A new candidate, named "IMEC-Clean" to potentially replace the RCA clean was later introduced, enabling near-perfect removal of metallic particles [8]. The IMEC-Clean includes a mixture of H₂SO₄/H₂O₂, followed by a 1% diluted HF. The use of H₂SO₄/H₂O₂ mixture was also demonstrated in the development of Nanowire Solar Cells to increase the conversion efficiency [9]. Development of interdigitated back contact (IBC) silicon solar cells was also enabled by a cost-effective cleaning mixture of H₂O/NH₃/H₂O₂ with various chemical concentrations and different cleaning temperature. Recently, the application of ozone in wet and dry semiconductor surface cleaning processes has gained significant attention. Ozone has been extensively used in waste and swimming pool water treatment, water purification, medical sterilization, odor control and many other industries, due to its strong oxidizing ability. A reliable ozone generation based on the dielectric barrier discharge was first developed by Werner Siemens in 1857 [10-12]. Since then it has become the standard ozone generation technique in

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^{*} Corresponding author.

many industries including water treatment and semiconductor processing. Chen discussed benefits and applications of ozonated deionized water (DI-O₃) for wafer surface preparation in detail [13]. DI-O₃ research has already been reported by a number groups [14–16]. Bakhshi et al. also demonstrated the use of DI-O₃ in surface preparation prior to the application of single or stacked dielectric layers such as SiN_x, AlO_x, and AlO_x/SiN_x. This has resulted in the outstanding surface passivation achieving the saturation current density J_0 of 8 fA/cm² (per side) [17]. In addition to wet ozone cleaning, dry ozone cleaning based on the exposure of ultraviolet radiation is less complicated to operate and is effective in removing a wide variety of contaminants from surfaces. The ability of UV ozone in removing the organic layer such as photoresist polymer was reported as early as 1972 [18]. In 1974 Sowell et al. presented the UV cleaning of adsorbed hydrocarbons from glass and gold surfaces, in air and vacuum environment [19]. Also, in 1974 John Vig and his team also described through a series of experiments that UV-ozone cleaning is capable of producing clean surfaces in less than a minute [20]. Chemically cleaned silicon surfaces (such as after HF process) are at risk of particle contaminations and absorption of hydrocarbon from the ambient air, organic resists, etc.; therefore passivating c-Si surface with a protective coating such as UV-ozone oxide significantly reduces contaminations and hydrocarbon absorptions [21]. Studies have shown that UV-ozone oxide treatment leads to a significant reduction of carbon content in the subsequently grown dielectric films [22,23]. Moldovan et al. also presented the use of UVozone to remove fingerprints and glue on the c-Si wafer surface, and that conditioning 70 Ω/\Box boron diffused layer with UV-ozone and passivating it with AlOx/SiNx stack achieved an emitter saturation current density of 49 fA/cm² [24]. The benefits of UV ozone have also been realized in organic photovoltaics. The use of UV-ozone to treat the ultrathin aluminum to form an alumina interlayer-between the active layer and indium tin oxide (ITO)-has been presented to improve electron extraction [25]. Treating the zinc oxide-poly vinyl pyrrolidone (ZnO-PVP) nanocomposite film used as an electron tunneling layer with UV ozone also improves the charge collections in dithienogermole-thienopyrrolodione-based polymer solar cells [26]. Besides the electron tunneling layers, treating the hole collection layer such as molybdenum trioxide (MoO₃) with UV ozone improves the surface morphology, transmittance and film quality [27]. Also, UV-ozone was demonstrated to change the highest occupied molecular orbital (HOMO) level of Phenyl-C61-butyric acid methyl ester (PC₆₁BM) [28]. In this paper, we present a novel method of cleaning the silicon surface by the UV-ozone technique in comparison to the industry standard RCA clean for application in silicon photovoltaics. We also employ a thin UV-ozone oxide (UVo) as an interface dielectric layer prior to the passivation of aluminum oxide (AlO_x) on c-Si samples. A deposition time of UVo interface dielectric was varied to optimize the passivation quality. We demonstrate that UVo technique is capable of providing both effective surface cleaning and outstanding passivation quality on c-Si silicon samples. In addition, we present a simple method to extract capture cross section values from already measured parameters of saturation current density J₀, interfacial trap density D_{it} and total fixed charge Q_{tot.}

2. Materials and methods

Planar 1–5 Ω cm n-type 250 μ m Cz wafers were used in this contribution. Saw damage silicon etch was processed in Tetramethylammonium hydroxide (TMAH) at 90 °C, removing approximately 1 μ m of silicon per minute. Effective carrier lifetime τ_{eff} and J₀ (per side) were measured using the transient photoconductance (PCD) decay technique at the excess carrier densities of 1×10^{15} and 5×10^{15} cm⁻³, respectively. The measurement of J₀ undertaken at the carrier injection level higher than τ_{eff} is due to the fact that at regions, where the excess carrier densities are far greater than the substrate doping, maximizes the range of carrier lifetime's linear dependence on

the carrier density, thereby distinguishing the surface from the bulk effects for the improved accuracy of J₀ analysis. J₀ is determined by the $\frac{qWn_i^2(\Delta n + N_d)}{2}(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{bulk}}), \text{ where } q \text{ is the electronic}$ relation of $J_0 =$ charge, W is the thickness of the silicon sample, n_i is the intrinsic carrier concentration, N_d is the bulk dopant concentration of the silicon sample, τ_{eff} is the effective minority carrier concentration and τ_{bulk} is the intrinsic bulk lifetime of crystalline silicon parameterized by Richter et al. [29]. Carrier lifetime represents bulk and surface recombination. Symmetrically passivated samples were used for measurement of τ_{eff} and Jo. RCA cleaning used a mixture of NH3:H2O2:H2O 1:1:5 and HCl:H₂O₂:H₂O 1:1:5 for the first and second cleaning step, respectively. UVo growth took place in Jelight 42 UV-ozone generator. In the ozone generator contaminant molecules and ozone absorb the short wavelength UV of 253.7 nm, and excite and simultaneously dissociate molecular oxygen at the wavelength of 189.9 nm. The photosensitized oxidation process happens when contaminant molecules react with atomic oxygen and so desorb from the surface. Recent technologies have made ozone cleaning process an extremely economical approach in both laboratories and industry. Using this technique, we have formed a thin layer of SiO_x on our samples. Dielectric layers (SiO_x, AlO_x, and RCA oxides) were removed in dilute (10%) HF prior to re-passivation. The thickness of UVo (or thin SiO_x) and AlO_x were measured by spectral ellipsometry (M-2000 J.A. Woollam) in a range of wavelength between 250 nm and 1200 nm. The measured signals are fitted using the Cauchy model. Based on the model, UVo oxides with the thickness of 1.5 nm, 1.7 nm, and 1.8 nm were achieved for 10 min, 15 min, and 20 min of process time, respectively. Deposition of AlO_x was by thermal atomic layer deposition (Cambridge NanoTech Savannah 100 ALD) with the deposition rate of 0.088 nm/Cycle at 200 °C. Annealing of UVo/AlOx passivated samples was processed in the nitrogen ambient at 450 °C for 30 min. A contactless capacitance-voltage (C-V) measurement technique using PV2000 Semilab SDI instrument was used to characterize Dit and Qtot. PV2000 tool dispenses charges on dielectric surface and measures surface voltage with vibrating Kelvin probe. Unless otherwise stated, D_{it} and capture cross section σ_n (or $\sigma_p)$ reported in this contribution represent the values near the midgap. D_{it} and Q_{tot}-based on the contactless CV measurement-have the measurement uncertainty of 2% and 1%, respectively; while τ_{eff} and J_0 have the reported uncertainty of 3% [30,31]. Finally, nano-scale interface characterization was carried out with the help of transmission electron microscopy (TEM). For this purpose, cross-sectional TEM specimens were prepared by focused ion beam (FIB) milling technique using a FEI 200 TEM FIB. High-resolution TEM (HRTEM) images were obtained with the help of FEI Tecnai F30 TEM system at an operating voltage of 300 kV with a point-to-point resolution of 0.2 nm.

3. Results and discussions

First, n-type $Cz < 100 > 1-5 \Omega$ -cm samples were processed in TMAH to remove saw damage, followed by cleaning them in RCA solutions to make the surface hydrophobic. Post-TMAH processed samples have resulted with $\sim 180 \,\mu m$ in thickness. Half of the samples were deposited with AlO_x having the thickness of 10–15 nm, while the rest were deposited with a very thin UVo (10 min of deposition) overlaid by the AlO_x of 10–15 nm. All samples were then annealed in N_2 ambient, followed by the PCD measurement. As shown in Fig. 1, the sample deposited by the UVo/AlO_x stack has notably improved τ_{eff} (i.e., 1554 μ s compared to 1019 μ s) and J₀ (7 fA/cm² compared to 11 fA/cm²) than that by AlO_x alone. The passivation quality in terms of an effective surface recombination velocity, Seff of the sample passivated by AlOx only in this experiment is 8 cm/s, somewhat comparable the published result of 5 cm/s [32]. Here, Seff is determined by the ratio of the wafer thickness to two times the τ_{eff} , assuming an infinite bulk lifetime time, as in published literature [32], and thus represents the upper limit. Typically, AlOx effectively passivates the c-Si surface by the Download English Version:

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