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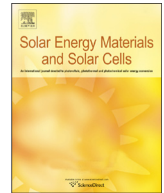
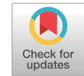


Review

Detailed structural and electrical characterization of plated crystalline silicon solar cells



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A R T I C L E I N F O

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A B S T R A C T

In this paper a detailed study on the electrical characteristics of Ni/Cu/Ag plated p-type Passivated Emitter Rear Contact (PERC) silicon solar cells is reported. By comparing the cell performance of different cell groups, pseudo Fill Factor (pFF) degradation by laser-induced defects, is observed. High-power (hard) laser ablated cells exhibit a lower efficiency and faster degradation with thermal ageing. We also present structural and electrical characterization to further visualize and identify the responsible defects, which turn out to be laser-ablation-induced dislocations, penetrating the silicon emitter and base. Increasing the laser fluence gives rise to a higher dislocation density. These dislocations are further confirmed as active generation-recombination centers by Deep Level Transient Spectroscopy (DLTS) analysis. The laser ablation induced dislocations are unavoidable because even at insufficient laser fluence (0.48 J/cm^2) to fully open the dielectric stack, the density is already at the level of 10^6/cm^2. A substitutional nickel peak is also detected by DLTS, suggesting nickel diffusing into the silicon base during the sinter step. Whereas no copper levels are found in the p-type silicon base by DLTS even after thermal aging at 235 °C.

1. Introduction

In recent years, developing an improved method for the metallization of silicon solar cells has been extensively studied. In the commercial solar cell market, the contact formation using Ag screen printing is the dominant technology as it is simple and suitable for mass production. However, this metallization has the disadvantage in having a low aspect ratio and high contact resistance therefore limiting the solar cell efficiency. The current trends with Ag screens involve using narrow opening width, smaller wire diameter and high opening fractions [1,2]. However, this reduces the screen lifetime and yields higher finger resistance as the printed amount is reduced. On the other hand, the advanced fine line printing techniques often require expensive screens and two-step printing, which lead to higher yield losses due to alignment needs and wafer breakage. All these factors of screen printing limit reductions in solar cell manufacturing costs. Besides that, Ag is an expensive and noble material and hence is subjected to a high price volatility. The mounting cost of silver pastes and decreasing silicon wafer thickness encourages silicon solar cell manufacturers to develop alternative metallization techniques that reduce the usage of Ag and get rid of the pressing process of screen printing while still having a compatible solar cell performance.

The plated Cu/Ni has been considered as one of the most viable candidates for future contact technology for silicon solar cells. A plated Cu/Ni contact is known to have a high conductivity and low contact resistance. Copper's conductivity is compatible with silver while its raw material cost is nearly a hundred times smaller [3]. This is an important factor for cost reduction compared to the current technology. On the other hand, Cu has been widely used in Si Ultra Large Scale Integration (ULSI) due to its low resistivity and good resistance to electromigration [4].

Therefore, the plated Cu/Ni contact scheme not only presents solution to the issues associated with Ag screen printed contacts but also shows absolute efficiency gain of 0.5% [5].

However, it is also well known that Cu is a fast diffuser into Si and can act as a deep level impurity [6]. The diffused Cu can form traps which reduce the carrier lifetime and increase the leakage current once they are present near a p-n junction. To prevent the Cu diffusion, a diffusion barrier, such as a plated Ni layer is often used between Cu and silicon [7–10]. The Ni silicide which forms by annealing has a low contact resistance and acts as adhesion layer. Using Ni/Cu plating techniques is a good solution to improve the cell efficiency also because

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of less shading loss. By using laser ablation to open the passivation layer before plating, it is possible to achieve a width of less than 15 µm. However, despite these advantages, a final acceptance by the c-Si Photovoltaic (PV) community for introducing Cu in solar cell processing can only take place after thorough reliability results and an estimation for the module's lifetime.

In this study, thermal ageing testing for the p-type PERC cells with shallow emitter and front Ni/Cu metallization is discussed. This is complemented by a characterization of the electrically active defects, based on Scanning Electron Microscopy (SEM) and effective lifetime measurements Bias Temperature Instability (BTI). The second part of the paper takes a closer look at the electrical characteristics of the cells before and after thermal ageing, using Deep Level Transient Spectroscopy (DLTS).

2. Experimental details

2.1. p-PERC device fabrication

In this work, large area (156 × 156 mm^2) p-type, 1–3 Ω cm, magnetic Czochralski (CZ) Si wafers, with starting thickness of 180 µm, were used. After random pyramid texturing for the front by KOH texture and inline rear polishing by HF/HNO_3, the wafers were processed according to the process sequence given in Fig. 2.

Prior to $POCl_3$ diffusion, the silicon wafers were subjected to a full Radio Corporation of America (RCA) clean in order to remove organic and metallic contamination before the fabrication process. A 2% HF solution was applied to remove phosphorus silicate glass, which formed during the $POCl_3$ diffusion step. After the Sulfuric Acid and hydrogen Peroxide Mixture (SPM)/HF clean, dry thermal oxidation was employed in order to drive-in phosphorus atoms in the Si bulk, forming thus a 0.5 µm deep homogeneous n^+ emitter with a sheet resistance of 120 Ω/sq and low surface concentration (Ns < 10^{20} cm^{-3}). Subsequently, the $POCl_3$ diffusion emitter was passivated with a Plasma-Enhanced Chemical Vapor Deposition (PECVD) SiN_x:H layer, and at the rear a PECVD SiN_x:H was applied on top of the CVD SiO_2 diffusion mask.

For the rear dielectric stack, contact opening was formed on all cells by Ultra-Violet (UV) (355 nm) nanosecond laser ablation with a fixed pitch of 500 µm and an opened diameter of approximately 30 µm. Subsequently, 2 µm of aluminum was deposited by physical vapor

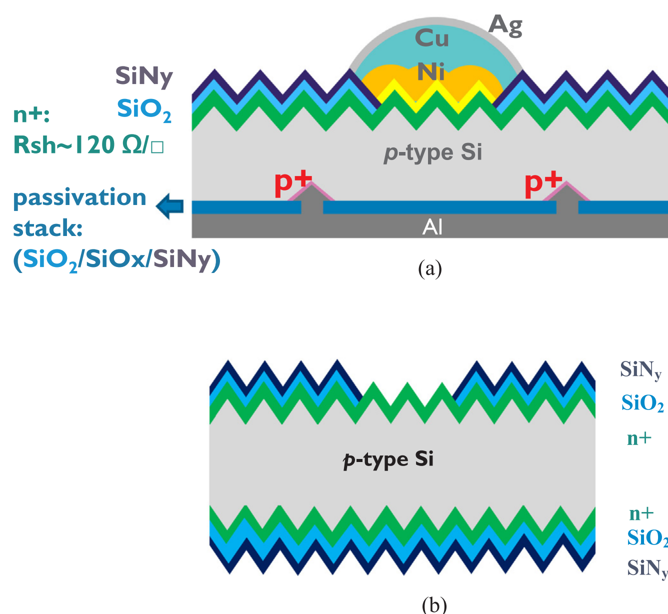

Fig. 1. (a) p-type PERC cell structure, (b) defect visualization and lifetime test structure.

Process sequence
Wafer 150mm, p-type, 1-3Ωcm, 160µm thick
KOH texture + rear polishing
Clean + $POCl_3$ diffusion
Rear emitter removal
Clean + Thermal Oxidation
PECVD SiN_x front
PECVD SiO_y/SiN_x rear
Ns-UV contact ablation rear
Al sputtering rear
Local Al-BSF formation (belt furnace)
H pattern front (ps UV laser ablation)
Ni/Cu/Ag plating + Sintering

Fig. 2. Process sequence for i-PERC cells.

deposition (PVD) onto the rear surface, followed by a firing step in an inline belt furnace resulting in a local Back Surface Field (BSF). This process sequence yields i-PERC (industry applicable Passivated Emitter and Rear Contact) solar cells.

The dielectric layer on the front (SiN_x:H) was opened by UV-ps laser ablation, the laser speed was kept the same for all the samples, only the laser fluence was changed: 0.69 J/cm^2 (soft laser) and 1.08 J/cm^2 (hard laser). Prior to plating, a short HF dip was performed to remove any native oxide in the contact opening areas. Approximately 1 µm of nickel was deposited by Light Induced Plating (LIP) followed by 8–10 µm of electroplated copper. Then the samples were immersed into a silver bath to form a thin silver layer in order to prevent oxidation of the copper. All the plating steps were performed in a commercial in-line plating tool from Meco [11]. Contact sintering was then applied for the full metal plated stack in a nitrogen ambient at 250 °C for few minutes to form a nickel silicide layer, reducing the contact resistance. The cross-section of the final p-PERC cell structure is shown in Fig. 1a.

In this work, thermal ageing, which is considered to be the most detrimental for Cu-based metallizations, is discussed. Ageing experiments are performed in vacuum ambient for temperatures up to 235 °C. Samples are intermediately removed from the oven and measured electrically at various times. They are considered failed if the electrical properties reduce to 95% of the original value. The cells were characterized based on light current-voltage (I-V) measurement and Suns V_{oc} measurements. The I-V data were obtained at 1-sun illumination on a WXS-200S-20 Wacom Electric Co tool. Cells were measured on a temperature controlled Cu block in full contact with the rear surface. Pseudo fill factors (pFF) were extracted from curves of suns versus open circuit voltage (V_{oc}) using Sinton Instruments SunsVoc tester [12].

2.2. Defect visualization and lifetime test structure

In order to characterize defects induced during the contact opening by laser ablation, defect etching is carried out and visualized by a Scanning Electron Microscope (SEM). The analysis has been performed on p-type Si after n^+ emitter formation, deposition of SiO_2 and SiN_x at the front, followed by laser ablation with various laser fluences: 0.48 J/cm^2, 0.63 J/cm^2, 0.72 J/cm^2, 0.96 J/cm^2 and 1.43 J/cm^2. The sample structure for defect inspection is shown in Fig. 1b. Conditions of the emitter doping and dielectric layer deposition were the same as for the

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