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Polyimide for silicon solar cells with double-sided textured pyramids

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ABSTRACT

Silicon solar cells incorporating double-sided pyramidal texture are capable of superior light trapping over cells with front-side only texture. However, increased surface area, roughness and exposed < 111 > crystal planes of textured surfaces not only causes increased recombination, but also makes cells susceptible to shunting through pinholes in the dielectric at the sharp peaks and valleys of the textured pyramids. A polyimide film as an insulating interlayer film is investigated to circumvent the tradeoff between improved light trapping, increased recombination and increased shunt paths. When applied at the rear of the interdigitated back contact silicon solar cell structure, the polyimide film provides an excellent electrical insulation (> 1000 MΩ of insulation resistance) and increases photocurrent (~ 1.1 mA/cm^2) owing to an increased rear internal reflectance. The polyimide is also compatible with metal annealing of passivating dielectrics such as silicon nitride. Optical simulation and experimental results are combined in a 3D semiconductor simulation (Quokka) to quantify the possible gain of implementing the double-sided texture in high efficiency silicon solar cells.

1. Background

High-efficiency silicon solar cells typically have a textured front surface and a planar rear surface [1–5]. The light trapping in these structures suffers from the first-pass light rays incident to the rear surface being reflected into the escape cone of a front pyramid and coupled out [6]. Numerous light trapping schemes have been investigated to redirect rays such that a smaller fraction is reflected into the escape cone. These include the tiler's pattern [6]; perpendicular grooves [6]; a honeycomb texture realized by isotropic etching [1]; plasmonic nanoparticles on the rear of the wafer-based silicon solar cell structure [7]; a simple prism pyramidal texture realized by mechanical grooving [8]; a pigmented rear reflector [9]; dielectric back scattering [10]; diffused reflectors including white paint, titanium oxide nanoparticles, white backsheets and silver mirrors [11,12]; and a random pyramidal texture via alkaline etch solution [13] with and without chemical rounding [14]. Of these, the last scheme is the most widely-used and well-established method in the fabrication of silicon solar cells. The application of random pyramidal double-sided texture (DST) on the front and rear of silicon solar cells has been shown to provide superior light trapping relative to silicon solar cells with a textured front and a planar rear, as it helps to randomize the direction of light within the cell thereby reducing the chance of escape [6,14]. Note, however, that the inclusion of rear pyramids is only preferable to planar when the rear internal reflectance R_{intR} is high; our simulations indicate that the threshold is $R_{intR} > 80\%$. As alkaline-assisted pyramidal texture is a relatively easy technique that is well-established in the PV industry, it offers a viable way to increase light trapping in crystalline silicon solar cells. Although rear texture also increases surface recombination and makes the rear surface more susceptible to shunting in cell structures such as interdigitated back contact (IBC) cells, using a chemical etch to round the rear pyramids mitigates those problems and higher cell efficiencies have been attained [15–21]; moreover, it has been concluded that when the etch duration is short, the chemical rounding has little influence on the overall light trapping [14]. In this paper, we present an investigation into the tradeoff between optical enhancement versus increased rear surface recombination and shunting for DST. The optical enhancement provided by different types of DSTs is examined via ray tracing. Recombination on pyramidal textured surfaces is investigated with plasma enhanced chemical vapor (PECVD) deposited silicon nitride (SiN_x). Incorporating polyimide (PI) as an electrically insulating film is introduced as a solution to the increased risk of recombination and shunts caused by DST in silicon solar cells. An investigation into its insulating quality, effects on carrier lifetime, and absorption in the polymer film is also presented. A comparison of cells with and without DST and PI is assessed by 3D Quokka simulation.

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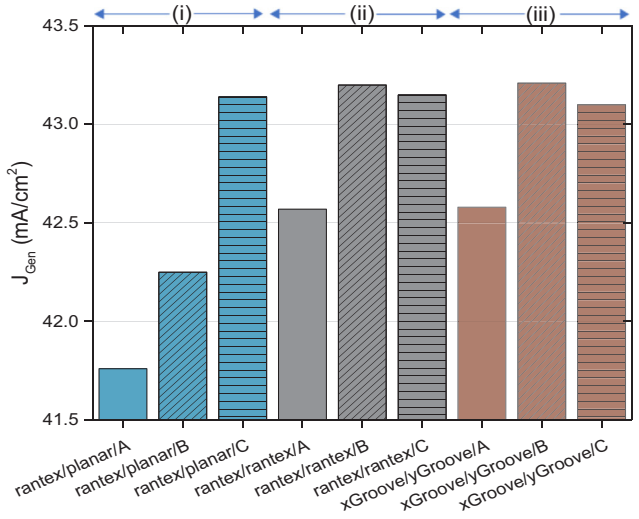

Fig. 1. J_{Gen} for a range of typical DST combinations. The parameters used are: normally incident AM1.5 G spectrum, a double-layer ARC (PECVD SiO_x and SiN_x of 80 nm and 75 nm, respectively) on the front surface, a 200 μm thick cell, and wavelength range of 300–1200 nm. Surface textures are referred to in the figure as 'rantex' for random pyramid texture, 'x grooves' for v-shaped grooves (52°) in 'x' direction, and 'y grooves' for v-shaped grooves (52°) in direction perpendicular to the 'x' direction. 'A' denotes that the internal reflection at the rear is specular and calculated for the case of films (a stack of 75 nm of SiN_x overlaid by 1000 nm of Al) coating the rear. 'B' denotes that the internal reflectance is 100% and specular. 'C' denotes that the internal reflectance is 100% reflection and Lambertian.

2. Optical enhancement of DST

Light trapping schemes in experimental high-efficiency silicon solar cells developed to date have had a textured front surface and a planar rear surface [2–5,22,23]. Numerous approaches have been presented to quantify the light trapping [6,24–31]. In the investigation carried out by Campbell and Green, the light trapping in silicon wafers was investigated for a number of structures such as (i) a textured front and a planar rear, (ii) pyramids on both sides, (iii) perpendicular grooves, (iv) a tiler's pattern and (v) a shifted brickwork pattern [6]. As an extension to this study, we apply the PV Lighthouse ray tracer [32] to simulate the photogeneration current density J_{Gen} for structures (i), (ii) and (iii). The results are presented in Fig. 1 and details of the input parameters are included in the caption. The choice of the front and rear surface morphologies that we present is motivated by their fabrication feasibility. A Lambertian rear surface is included to represent an "ideal" rear surface scenario.

Consistent with [6], who evaluated the case of specular and 100% reflectance from the rear (Case B), we find that the perpendicular grooves yield the greatest advantage over a rantex/planar structure ($\Delta J_{Gen} \sim 1$ mA/cm^2), but it is still only slightly superior to rantex/rantex, and this advantage is similar to that attained when the rear surface is Lambertian (Case C). We also find that when accounting for the rear films (Case A), ΔJ_{Gen} of these textures is reduced to ~ 0.8 mA/cm^2. Simulations with alternative dielectric materials (e.g., SiO_2, AlO_x, Si_3N_4) yielded similar trends. Thus, given the simplicity of its fabrication, rantex/rantex appears an excellent candidate for DST in commercial and laboratory silicon solar cells.

3. Application of DST with polyimide

Unfortunately, the benefit of improved light trapping by DST is offset by an increase in recombination due to its greater surface area, its sharp peaks and troughs, and (for some dielectrics) an exposure of < 111 > facets [33–36]. Thus, the ultimate benefit to solar cells depends strongly on the quality of the passivation. Two well-known and highly passivating films are PECVD SiN_x and ALD AlO_x, but these films do not provide robust insulation between metal and silicon substrate, and they are not suitable to be used as an insulating layer between the metal and textured or diffused silicon due to high leakage currents and low dielectric breakdown voltage [37]. This can lead to a poor shunt resistance and an increase in recombination. Shunting is also one of the major obstacles resulting in poor conversion efficiency in research and manufacturing of high efficiency IBC silicon solar cells [38]. We therefore explore the use of polyimide (PI) as an insulation layer between the metal and the dielectric films, testing its insulation properties and its effect on surface passivation and optics.

3.1. Polyimide

Polyimide (PI) films have been used as stress buffer layers, interlayer dielectrics, and protecting films in microelectronic applications [39–41]. PI films also have excellent mechanical properties allowing them to survive the thermal and chemical exposures of post-application processing, good elongation property that prevents cracking, and excellent adhesion to a wide range of metals. In addition, PIs are patternable by photolithography [42,43] and have been demonstrated as an interlayer dielectric for double-level metallization [44]. The PI films discussed herein appear to be well-suited as interlayer insulators between textured pyramids coated by low temperature passivation dielectrics and the rear metal.

3.2. Electrical insulation

The insulation capability of PI (HD-4100) was investigated by fabricating a heavy phosphorus diffusion (40 Ω/□) on symmetrically textured low-resistivity (1.5 Ω-cm) ~ 250 μm thick n-type silicon, and spin-coating 2–3 μm of PI onto the front side at 5000 rpm for 30 s and curing it at 350 °C in nitrogen for 30 min. Aluminum (Al) pads (~ 1 μm thick and 1 cm^2) were then evaporated on both sides of the sample, followed by sintering the samples in a forming gas environment at 250 °C for 30 min to ensure the Al was alloyed with the phosphorus-doped silicon at the rear. The presence of the heavy phosphorus diffusion ensured the contact resistivity between the Al and silicon substrate at the rear was negligible. The current-voltage characteristics were then measured using the 4-point probe method, contacting positive polarity probes to the Al pad on top and negative probes to the pad on the rear or vice versa to determine the total resistance. The average resistance measured across six test structures was ~ 7.7 × 10^9 Ω with a standard deviation of 3 × 10^9 Ω. In comparison, an insulation provided by a stack of SiO_2 and LPCVD Si_3N_4 films on interdigitated back contact cell structures [3,45–51] has an average resistance of ~ 1 × 10^7 Ω. The very high resistance of the PI film suggests that it is well-suited as an insulation layer between metal and textured pyramids.

3.3. Surface recombination

We employed undiffused high-resistivity n-type FZ < 100 > 100 Ω-cm silicon wafers that were textured with random upright pyramids and passivated with PECVD SiN_x (~ 75 nm). The J_o measurements were determined by a photoconductance decay (PCD) instrument following the Kane and Swanson technique [52], assuming an intrinsic carrier concentration of $n_i = 8.95 \times 10^9$ cm^{-3} (at 297 K). The measured J_0 was 7 fA/cm^2 (per side), which is typical of high-performing dielectric passivation on texture [33,34,36].

The PI film was then applied on both sides of the SiN_x coated samples at 5000 rpm for 30 s, followed by annealing in a nitrogen ambient at 300 °C, 325 °C, and 350 °C for 30 min and 60 min. The purpose of the nitrogen anneal is to mimic the imidization of PI film following the cure. Imidization refers to the conversion of a polyimide into an imide by heat (or a catalyst) through the reaction process that