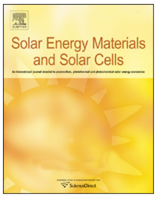
Solar Energy Materials and Solar Cells 182 (2018) 178–187

Contents lists available at ScienceDirect

Solar Energy Materials and Solar Cells

journal homepage: www.elsevier.com/locate/solmat



# Homo-heterojunction concept: From simulations to high efficiency solar cell demonstration

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## ARTICLE INFO

*Keywords:*
Heterojunction solar cells
Boron implantation

## ABSTRACT

The novel solar cell architecture called silicon homo-heterojunction (HHJ) cell is investigated combining experimental and simulation approaches. This structure intends to overcome the limitations of the silicon heterojunction technology regarding the amorphous/ crystalline silicon interface *(p)* a-Si:H/*(i)* a-Si:H /*(n)* c-Si) by the addition of a $(p^+)$ c-Si layer at the hetero-interface. First, the added $(p^+)$ c-Si layer is experimentally investigated using boron implantation through the realization and characterization of symmetric solar cell precursors. An adapted process flow taking into account the $(p^+)$ c-Si profile optimization, the annealing effects on substrate degradation, and the impact on surface passivation, is deeply explored. Then, large area solar cells are processed and the solar cell performance are discussed in view of the data obtained on precursors and with the help of realistic numerical simulations. Overall, we observe that the HHJ solar cells exhibit a small performance improvement compared to reference heterojunction cells. In particular, a gain in the fill factor is observed, which is shown to be originated from both an improvement in field effect and a decrease of the vertical series resistance from the a-Si:H layers. The experimental data obtained on the processed homo-heterojunction solar cells confirm that this technology can lead to improved conversion efficiencies compared to the high quality reference heterojunction solar cells.

## 1. Introduction

Amorphous/crystalline silicon (a-Si:H/c-Si) heterojunction solar cells (SHJ) have already demonstrated to be a promising alternative to standard homojunction solar cells in terms of efficiency but also in terms of industrial production and cost [1,2]. In 2012, numerous laboratories and companies have strongly improved efficiencies and succeeded obtaining n-type SHJ solar cells with power conversion efficiencies above 21% [3–7]. Moreover, results obtained in 2015 and 2016 by Kaneka surpassed the world record for crystalline silicon solar cells with more than 25% conversion efficiency (25.1% [8] and 26.7% [9,10] on large area regular and back contacted SHJ cells configurations, respectively) confirming the high potential of such structures for high efficiency cells and modules. The key of the SHJ technology is a simple and low temperature (< 200 °C) process based on the deposition of a-Si:H layers onto a c-Si wafer used both to passivate the surface and to build the front junction and back surface field allowing for extremely high $V_{OC}$ [11].

However, in today's SHJ solar cells, the a-Si:H/c-Si interface passivation on the emitter side is identified as one of the most important issue [12,13] limiting the SHJ cells performance specially because of the fill factor (FF)/open-circuit voltage ($V_{OC}$) compromise. Indeed, the passivation of the surface (limiting the device $V_{OC}$) is strongly enhanced by the use of an intrinsic *(i)* a-Si:H layer. However, such layer is resistive and impacts negatively the fill factor (FF) increasing vertical series resistances when increasing the thickness, while also impacting the short circuit current due to parasitic absorption, especially in the front emitter configuration. Thus, the *(i)* and *(p)* a-Si:H layer thicknesses are optimized for the compromise between passivation (low interface defect density $D_{it}$), doping (strong field effect) and vertical conduction. Additionally, the role of the transparent conductive oxide (TCO) [14,15] is required to collect laterally the charges (to insure low lateral series resistances) and to achieve an effective Metal/TCO/*(i/p)* a-Si:H/c-Si contact (correlated to vertical series resistance) [16].

Different approaches have been proposed to improve the passivation/field effect compromise, for instance, improving cleaning [13],

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https://doi.org/10.1016/j.solmat.2018.03.027
Received 1 September 2017; Received in revised form 19 February 2018; Accepted 13 March 2018

tuning the *(i)* a-Si:H layers structures and properties [17,18] or band management modifications using silicon based amorphous alloys [19–22].

An alternative option to improve the field effect is by the addition of a thin and highly doped *($p^+$)* c-Si region underneath the *(i)* a-Si:H passivation layer modifying the crystalline silicon space charge region. The resulting structure is called a homo-heterojunction (HHJ) for it combines a homojunction profile to improve band bending and vertical carrier collection with the amorphous hetero-emitter.

In previous numerical simulation studies [23], it was shown that, compared to the SHJ cell, the HHJ cell exhibits a higher open-circuit voltage and is less sensitive to interface defects. These features have been evidenced to originate from the additional field effect passivation brought by the *($p^+$)* c-Si region. Additionally, the HHJ cell fill factor is also improved and less influenced by interface defects [23]. Such improvements were also observed by simulations by other authors on similar homo-heterojunction cells with insertion of a highly doped crystalline layer at the emitter of either n-type or p-type silicon solar cells [24,25].

Concerning experimental results, the HHJ cells fabricated so far did not succeed to surpass the performance of SHJ cells because of their lower $V_{OC}$ due to increased recombination after the *($p^+$)* c-Si processing [26,27]. Such increased recombination could take place in the strongly doped *($p^+$)* c-Si region or could originate from a low *($p^+$)* c-Si/*(i)* a-Si:H chemical passivation. They can also appear in the substrate due to the creation of additional defects related to the high temperature needed for the *($p^+$)* c-Si layer processing (epitaxy, post-implantation annealing or diffusion) [28].

In this work, we use boron implantation to produce the *($p^+$)* c-Si layer. In a first part, ion implantation parameters are optimized using effective lifetime measurements on symmetrical *($p^+$)* c-Si/*(n)* c-Si/*($p^+$)* c-Si samples. Then, in a second part we fabricate HHJ cells and standard SHJ cells. For the first time we were able to obtain HHJ cells exhibiting slightly improved conversion efficiencies compared to the SHJ ones. Results are discussed and explained in the light of further numerical simulations.

## 2. Experimental details

### *2.1 Symmetrical $p^+np^+$ samples*

Symmetrical *($p^+$)* c-Si/*(n)* c-Si/*($p^+$)* c-Si samples ($p^+np^+$) are first processed by implanting boron (B) with a beam-line Varian VIISta® HCP implanter in 160–180 µm thick n-type textured Cz pseudo-square 156 × 156 cm$^2$ c-Si substrates with initial resistivity ranging from 3.0 to 4.0 Ω cm. Various energies and doses have been tested to obtain different profiles. In particular, c-Si wafers have been taken from the second quarter of the Cz ingot to avoid strong oxygen and metallic impurities known to be detrimental for substrate lifetime when high temperature steps are used during processing [29]. After an HF-$O_3$ cleaning step, boron is activated around 950 °C during 15 min in a nitrogen atmosphere. Such low activation temperature has been chosen following a previous work in order to limit bulk substrate damages [28]. By comparing the secondary ion mass spectroscopy (SIMS) results (Fig. 1) with that of electrochemical capacitance-voltage (ECV) (not shown here), the boron atoms were checked to be fully active [30]. Implantation parameters, boron dose and boron surface concentration deduced from SIMS are summarized in Table 1 for five batches ($HHJ_1$-$HHJ_5$), each batch consisting in three wafers.

Subsequent to the annealing step at 950 °C, *($p^+$)* c-Si surfaces are passivated using different stacks and layers:

- a 8/72 nm-thick $AlO_x/SiN_x$:H stack, deposited by atomic layer deposition (ALD) in a Beneq equipment at room temperature and high temperature plasma enhanced chemical vapor deposition (PECVD) in a Centrotherm tool at 450ºC, respectively,

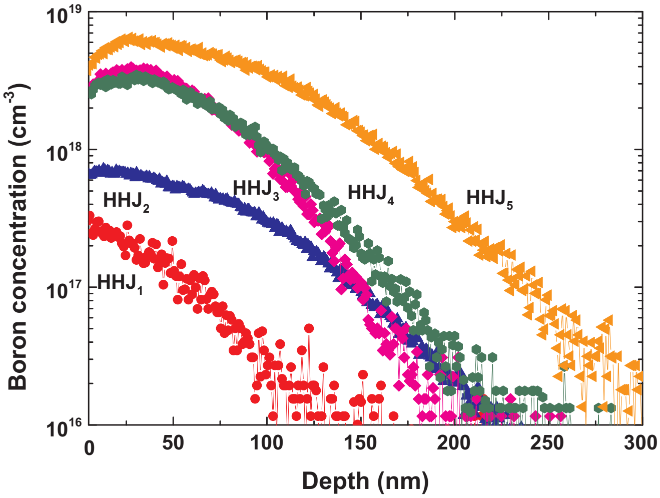

**Fig. 1.** SIMS measurement of the studied boron implantation profiles, on polished n-type c-Si substrates.

**Table 1**
Summary of implantation energy and dose conditions tested in this work, with measured boron dose and surface concentration from SIMS measurements after the annealing and the surface cleaning steps, and the corresponding calculated sheet resistance. These values are valid for polished n-type substrates. For textured substrates the implantation dose is multiplied by 1.7 in order to obtain similar sheet resistance from the implanted doped region.

| Batch name | Implantation energy kV | Implanted B dose cm$^{-2}$ | Measured B dose cm$^{-2}$ | $[B]^{surface}$ cm$^{-3}$ | $R_{sh}$ (Calculated from SIMS) Ω /□ |
|---|---|---|---|---|---|
| $HHJ_1$ | 1 | $1.0 \times 10^{13}$ | $1.7 \times 10^{12}$ | $4.0 \times 10^{17}$ | $1.4 \times 10^{4}$ |
| $HHJ_2$ | 10 | $1.0 \times 10^{13}$ | $1.0 \times 10^{13}$ | $7.5 \times 10^{17}$ | $4.2 \times 10^{3}$ |
| $HHJ_3$ | 1 | $1.0 \times 10^{14}$ | $3.1 \times 10^{13}$ | $3.0 \times 10^{18}$ | $1.7 \times 10^{3}$ |
| $HHJ_4$ | 5 | $5.0 \times 10^{13}$ | $3.0 \times 10^{13}$ | $3.0 \times 10^{18}$ | $1.7 \times 10^{3}$ |
| $HHJ_5$ | 10 | $1.0 \times 10^{14}$ | $7.3 \times 10^{13}$ | $5.0 \times 10^{18}$ | $8.5 \times 10^{2}$ |

- a-Si:H layers deposited at 200 °C by PECVD in a Jusung cluster tool :

o a 18 ± 1 nm thick *(i)* a-Si:H layer,
o a 20 ± 1 nm thick *(i/p)* a-Si:H stack,

It is already known that thanks to the $AlO_x$ negative charges, the $AlO_x/SiN_x$:H stack passivates very efficiently B-doped c-Si surfaces [31] and will serve as our passivation reference. The *(i/p)* a-Si:H stack is the same as used in SHJ solar cells at INES [8] and will be used for the realization of HHJ cells.

For comparison purposes, we also processed two other batches of symmetrical structures, that we designate as $SHJ_{REF}$ and $SHJ_{950\,°C}$ in the following. These are reference samples without any boron implantation and using the standard cleaning procedure developed at INES for the fabrication of silicon heterojunction solar cells [8], except that $SHJ_{950\,°C}$ has been submitted to the same annealing step at 950 °C as the HHJs samples (before deposition of the surface passivation layers) in order to investigate the effect of such annealing on the wafer properties.

Injection dependent effective minority carrier lifetime curves are obtained using a WCT-120 Sinton Instrument setup. For an easy and rapid comparison these curves can be used to extract the effective lifetime at an injection level of $10^{15}$ cm$^{-3}$ [32] or the implied open-circuit voltage (i-$V_{OC}$) [33].

For samples with the *(i/p)* a-Si:H passivation stack, we also deposited top co-planar electrodes made of a bi-layer of indium tin oxide (ITO) covered with silver, with various interspacing distances. We the applied the transfer length method (TLM) in order to get insight into