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Properties of mixed phase silicon-oxide-based passivating contacts for silicon solar cells

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ABSTRACT

We investigate the properties of an electron selective front contact based on a phosphorous doped mixed-phase SiO_x/Si layer stack at device level. The addition of the SiO_x phase to the Si layer targets reduced optical absorption, pursuing the goal of a broad-band transparent full-area passivating contact for front-side application. To demonstrate the validity of our approach we realised a planar hybrid solar cell with the mixed-phase SiO_x/Si-based passivating contact on the front side and a hydrogenated amorphous (i/p) silicon heterojunction as rear hole-selective contact. With this structure, we obtained a V_{OC} of 691 mV, a J_{SC} of 33.9 mA/cm^2, a fill factor of 79.4% and an efficiency of 18.6% on a planar n-type FZ Si-wafer.

Temperature-dependent *IV*-measurements at solar cell level were performed in order to understand the physical mechanisms behind charge carrier transport and surface passivation of the mixed-phase SiO_x/Si layer stack. The results were compared to those of a standard silicon heterojunction (SHJ) cell on a similar planar substrate. The temperature dependence of the *IV*-curves in the range from –100°C to +75°C reveals that the hybrid cell is less temperature sensitive with respect to the SHJ cell. Furthermore, at low temperatures, the analysis reveals a reduction of the V_{OC} temperature coefficient of the hybrid cell, whereas for the SHJ cell a saturation occurs. This behaviour hints that the barrier imposed by the SiO_x/Si-based contact is less pronounced than the barrier imposed by a standard SHJ contact.

1. Introduction

Crystalline silicon (c-Si) solar cells currently account for more than 94% of the overall photovoltaic cell production [1], making them a key technology to replace conventional energy sources such as nuclear power, fossil fuels or gas. To increase the conversion efficiency of c-Si cells further, it is necessary to suppress minority charge-carrier recombination losses at the interfaces between the Si-absorber and the electrodes, while still maintaining efficient majority charge-carrier extraction [2,3]. Minority charge-carrier recombination can be reduced with dedicated passivation and contacting schemes, which prevent a direct contact between the silicon absorber and the metallisation [4]. Recently, passivating contact technologies, such as tunnel oxide passivated contacts (TOPCon), polycrystalline silicon on oxide (POLO) or poly-Si based passivating contacts on thin oxides have shown excellent carrier selectivity and passivation properties [5–9]. However, because of their parasitic absorption, they have been so far mainly applied to the rear side of solar cells. Such passivating contact technologies consist of a highly doped silicon-based layer deposited on top of a thin (typically <2 nm) silicon oxide (SiO_x) buffer layer. A doped region in the crystalline Si absorber is created during a thermal annealing step by in-diffusion of dopants through the thin oxide layer from highly doped deposited layers. The doped region has different conductivities for holes and electrons, and therefore enhances charge-carrier selectivity [2,3,10]. In addition, the thin SiO_x layer at the c-Si wafer surface reduces the density of electronic surface defects.

With excellent passivating junctions for the rear, the front side contacting scheme becomes the limiting factor to achieve high efficiencies. In order to extend the applicability of passivating contacts to the front side, they have to meet additional requirements. Besides providing good passivation behaviour and transport of the selected charge carrier type, front-side schemes should be preferably highly transparent in order to avoid parasitic absorption losses. Furthermore, the advantage of applying passivating contacts over the full wafer area

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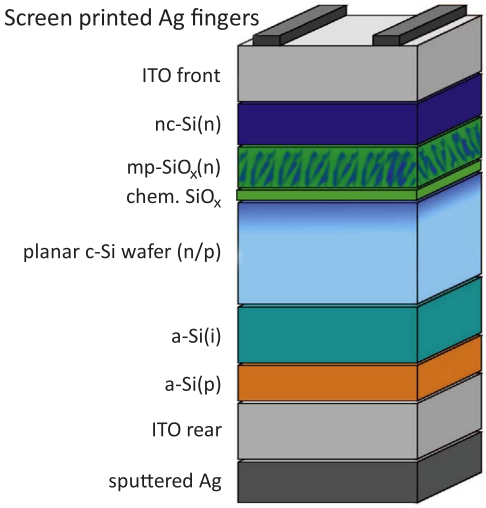

Fig. 1. Schematic of the hybrid cell architecture for testing the mp-SiO_x(n)/nc-Si(n) stack as front-side passivating contact. An a-Si(i/p):H rear emitter is used in this configuration. The darker region in the wafer just below the chem. SiO_x indicates the in-diffused n^+-region.

is that complex patterning steps are no longer needed. To meet all those requirements, we have developed a passivating contact layer stack that consists of a mixed-phase material comprising conductive inclusions of silicon embedded in a matrix of silicon oxide [11]. Our layer stack is prepared by depositing a phosphorus-doped double layer, consisting of a mixed-phase SiO_x (mp-SiO_x(n)) and a nano-crystalline silicon (nc-Si (n)), followed by a thermal annealing step. A first planar proof-of-concept solar cell with the mp-SiO_x(n)/nc-Si(n) front passivating contact was presented recently [12,13]. While replacing part of the nc-Si by mp-SiO_x reduces the effective absorption, it may introduce transport barriers [14].

In this paper, we investigate the transport properties of the full-area front-side electron selective mp-SiO_x(n)/nc-Si(n) contact layer at device level. For this, we have implemented the contact in a planar hybrid solar cell with a heterojunction hole-selective rear contact (see Fig. 1). We use temperature-dependent *IV* measurements of the hybrid devices and a heterojunction sister samples to draw conclusions about the transport properties of the mp-SiO_x(n)/nc-Si(n) contact.

2. Experimental

The mp-SiO_x(n)/nc-Si(n)-based passivating contact was investigated using symmetric lifetime samples as described in detail in [11] and [13]. These were prepared on 200-µm-thick 4-in. (100) phosphorous-doped float zone silicon wafers with resistivity of 10 Ω cm or 1 Ω cm. The wafers were cleaned using standard wet chemistry and covered by a thin chemical oxide layer (chem. SiO_x) using an aceotropic HNO_3/H_2O mixture at 80°C [15,16]. Subsequently, a highly phosphorous-doped mp-SiO_x(n)/nc-Si(n) stack was deposited by plasma enhanced chemical vapour deposition (PECVD). The PECVD depositions were followed by thermal annealing in nitrogen (N_2) atmosphere for 15 min at a temperature of 900°C. During the thermal anneal, the layers crystallise partially and a highly phosphorous-doped region (darker region of c-Si substrate in Fig. 1) is formed in the topmost region of the c-Si wafer by in-diffusion of phosphorous through the thin SiO_x layer from the mixed phase layer stack. Surface passivation was enhanced by hydrogenation of the wafer/chem. SiO_x interface by annealing the samples at 500°C for 30 min in forming gas (FGA) consisting of 4% H_2 diluted in N_2.

For device fabrication, the mp-SiO_x(n)/nc-Si(n) stack was applied only on the front side of n- and p-wafers, and the rear side was either coated with a protective silicon oxide or not intentionally coated further. After annealing, the silicon oxide layer (protective or thermal) on the rear side was removed with 5% hydrofluoric acid (HF). Then, a hole-selective heterojunction consisting of intrinsic amorphous silicon (a-Si:H) and boron-doped a-Si:H(p) was deposited by PECVD on the rear side. After a short dip in 1% HF, a magnetron sputtered ITO (indium tin oxide) layer was applied to the front side (thickness 142 nm with 50 Ω/□ sheet resistance or 81 nm with 360 Ω/□) through a shadow mask. For the rear side an ITO layer (thickness 130 nm and 170 Ω/□ sheet resistance) and a metallic silver (Ag) reflector were deposited by magnetron sputtering. The cells were finished by screen printing a silver grid on the front and by finally curing them for 30 min at 210°C in a belt furnace. To define the active cell area, the ITO/Ag rear stack was deposited through an aligned shadow mask.

The structure of the contact layer stack after annealing was analysed by scanning transmission electron microscopy (STEM). For that purpose, thin lamellae were extracted using the conventional focused ion beam (FIB) lift-out method in a Zeiss NVision 40, employing a final gallium ion milling voltage of 2 kV. STEM high-angle annular dark-field (HAADF) images were acquired in combination with energy-dispersive (EDX) and electron energy-loss (EEL) spectra in a FEI Titan Themis microscope, which was operated at 200 kV with a beam current of 100 pA. The convergence semi-angle was set to 28 mrad, while the collection semi-angle of the EELS spectrometer was 48 mrad.

The samples were characterised after the different process steps by injection dependent photo-conductance decay (PCD) lifetime measurements to obtain the minority carrier lifetime (τ_{eff}), as well as the resulting implied open-circuit voltage (iV_{OC}) [17]. For the final cells, the current-voltage (*IV*) curves were measured at 25°C with a source meter (Keithley, 2601A), using an AAA solar simulator (Wacom) set to 100 mW/cm^2 with a calibrated c-Si solar cell. The External Quantum Efficiency (*EQE*) and the reflectance (*R*) were measured with an *IQE*-Scan from PV-tools. From those measurements, the wavelength-dependent Internal Quantum Efficiency (*IQE*) was calculated. For the temperature-dependent *IV(T)*-measurements an in-house built hybrid light-emitting diode (LED)-halogen solar simulator with a temperature-controllable chuck was used in the temperature range of –100°C to +75°C. Detailed information about this set-up can be found in [18]. The illumination intensities and the spectrum of this setup are not perfectly calibrated, as the distance between light source and chuck was increased and an additional glass pane was introduced to enable temperature measurement down to –100°C. Therefore, it is possible to compare different samples, but absolute values will slightly differ from calibrated *IV*-measurements performed with a sun simulator (Wacom, class AAA) at 25°C.

3. Results and discussion

3.1. Structure of the mp-SiO_x(n)/nc-Si(n) passivating contact

In previous studies, we have investigated and optimised our mixed-phase mp-SiO_x(n)/nc-Si(n) passivating contact layer stack by preparing symmetrical lifetime samples. The influence of annealing temperature, annealing time and doping concentration are described in [11,13].

To investigate the structural properties of the mixed-phase mp-SiO_x(n)/nc-Si(n) passivating contact layer, STEM HAADF images were acquired in combination with EDX and EEL spectra on a sample annealed at 900°C for 15 min (Fig. 2(a)–(c)). The low-loss EEL spectra were processed using the methodology reported in [19] and [20] to distinguish the Si-rich regions from the ones containing SiO_x. The method relies on the difference in plasmon response between Si and SiO_x. The sharp Si plasmon peak is highlighted by subtracting from its average intensity (15.5–19.5 eV) a background extrapolated from the energy losses at 8–12 eV and 21–25 eV. Bright regions are Si rich, while darker regions are richer in SiO_x (Fig. 2(c) and (d)).

While also apparent in the HAADF (a) and EDX map (b) of Fig. 2, the thin chemical oxide can be clearly distinguished as a dark layer in