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Advanced light management techniques for two-terminal hybrid tandem solar cells

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ABSTRACT

Multi-junction solar cells are considered for various applications, as they tackle various loss mechanisms for single junction solar cells. These losses include thermalization and non-absorption below the band gap. In this work, a tandem configuration comprising copper-indium-gallium-di-selenide (CIGS) and hydrogenated amorphous silicon (a-Si:H) absorber layers is studied. Two main challenges are addressed in this work. Firstly, the natural roughness of CIGS is unfavorable for monolithically growing a high quality a-Si:H top cell. Some sharp textures in the CIGS induce shunts in the a-Si:H top junction, limiting the electrical performance of such a configuration. To smoothen this interface, the possibility of mechanically polishing the intermediate i-ZnO layer has been explored. The second challenge that is addressed, is the significant current mismatch in these tandem architectures. To enhance absorption in the current-limiting top cell, the ZnO:Al front electrode was textured by means of wet-etching the entire tandem stack. We demonstrated that one can manipulate the morphology of the random textures by varying the growth conditions of the ZnO:Al, leading to better light management in these devices.

1. Introduction

Thin-film technologies can have certain attractive characteristics in terms of weight, shapes, and possible translucence. In search for higher voltages and efficiencies, much research has focused on multi-junction thin-film photovoltaic devices. This is not limited to the field comprising III-V semiconductors, but also thin-film technology materials have been extensively researched. Combining a-Si:H with nanocrystalline silicon – the micromorph solar cells – has widely been investigated [1], but also work on (all silicon-based) triple-junction [2] and even quadruple junction solar cells are found in literature [3,4]. Likewise, multi-junction configurations are considered in the field of organic photovoltaics [5,6]. Beyond that, merging of different photovoltaic technologies in so-called hybrid multi-junctions is also being explored. Recent development are found in combining one junction of crystalline silicon with a junction of perovskite [7] or III-V semiconductors [8]. In addition, in the field of CIGS such stacks have been proposed, including combining this junction with various dye sensitized solar cells [9–11]. In this latter field, an additional incentive is to limit the use of the relatively scarce Indium. Using multi-junction devices, thinner CIGS layer can generate higher photo-conversion efficiencies, due to both higher voltages obtained in thinner absorber layers [12,13], as well as the better spectral utilization.

In terms of contact and interconnection design, multi-junction devices can be categorized in two configurations; two-terminal and four-terminal devices. The challenge for four-terminal multi-junction devices lies in the complex electrical components required for the integration of these cells in modules and complete systems. The challenge for two-terminal devices is to accomplish a design in which top cell and bottom cell are close to current matching while preserving a high value for the fill factor *(FF)*. Consequently, two-terminal configurations face the biggest challenges in the design and fabrication of the cells.

This work focuses on two-terminal double-junction devices, where all layers are monolithically integrated. In these devices, two PV cells based on semiconductor absorber layers with different energetic bandgaps are stacked, with the cell based on the widest bandgap material facing the front side at which the irradiance is incident. In such a tandem cell the photons have - on average - less excess energy relative to the bandgaps, reducing thermalization losses, and thereby resulting in a more efficient utilization of the solar spectrum.

CIGS is a direct bandgap material with a high absorption coefficient till close to its band gap around 1.2 eV. This makes CIGS a suitable semiconductor material to function as a bottom cell in these devices. The amorphous silicon solar cell technology regards a wide bandgap

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material (1.66 eV), is well-developed, and is processed at a temperature below 200 °C. These properties making a-Si:H a suitable candidate for use as top cell in this configuration.

The integration of these CIGS and amorphous silicon cells in one monolithic stack faces several challenges. First of all, in conventional single junction amorphous silicon and micromorph solar cells illumination through the p-doped layer is favorable, as these cells are constraint by the drift length of the holes. In this novel device structure, the a-Si:H top cell is to be illuminated through the n-doped layer to align it with the configuration of the CIGS. Secondly, it is challenging to grow high-quality a-Si:H layers on the rough CIGS. The relatively sharp texture results in a-Si:H cell with a high shunt density. In addition, the amorphous silicon cell is current limiting. Increasing the light absorption of the top cell can significantly improve the performance of the tandem cell.

In this work, we demonstrate two approaches to tackle the above limitations to improve the performance of a-Si:H/CIGS tandem device. In the first approach, the CIGS cell is smoothened by mechanical polishing the ZnO interface. The smoother CIGS half fabricate facilitates the growth of a shunt-free a-Si:H top cell, increasing the V_{oc} and fill factor of the tandem cells. Very little related research to this methodology of interface smoothening can be found in literature. This concept has previously been demonstrated for micromorph solar cells where an intermediate i-ZnO layer [14] or nanocrystalline SiO_x:H [14–16] has been polished. An extensive study of polishing ZnO built the framework for this research [17]. Mechanically polishing of layers on top of CIGS solar cells is unprecedented. Such smoothening approach induces additional challenges in terms of optimization, due to relative weak semiconductor-metal bonding.

The second approach is based on texturing of the ZnO:Al front electrode to enhance the generated photocurrent in the top sub-cell by forward scattering. Texturing of TCOs is a well-known strategy for light management in photovoltaic devices [18,19]. In this work, a wet-etching procedure is used for creating a textured front TCO surface. When a TCO is subject to an acid, the acid starts to react with the material, along its surface. Due to the columnar growth of TCOs, the acid will also penetrate partially along the grain boundaries and voids and etch the bulk of the material. Due to etching along the increased surface area at the grain boundaries, a inhomogeneous lateral etching speed is realized and a textured surface is realized. Likewise, when the acid penetrates and etches inside the voids, these develop into relatively larger craters. Wet-etching a TCO using this procedure, creates random textures that induce light scattering and improve light incoupling. By varying the type of TCO, deposition parameters, and etchants, one can alter the type of textures.

2. Methodology

2.1. Fabricating bottom sub-cell

The half fabricate comprises the glass substrate, molybdenum back contact, CIGS absorber layer, CdS buffer layer and the intrinsic ZnO (glass/Mo/CIGS/CdS/i-ZnO). A 1 mm thick sodalime glass substrate was cleaned in five steps. Firstly, it was scrubbed clean using isopropanol on tissue, followed by immersion in 4 consecutive baths of 10 min; first an ultrasonic bath of acetone; secondly an ultrasonic bath of isopropanol, followed by two baths of HNO_3 (a 99% HNO_3 bath at room temperature, and a 69% HNO_3 bath at 100 °C). After these steps the substrates are extensively rinsed with de-ionized water (DI water).

A 420 nm layer of molybdenum was sputtered on this substrate in two pressure steps. First, a more porous layer to adhere well to the substrate was deposited, followed by a more dense layer to form a well-conducting back contact. A 1 μm CIGS was deposited using three-stage-*co*-evaporation. During the CIGS deposition, the sodium diffuses into the CIGS layer through natural diffusion from the substrate. The first stage was processed at 400 °C, stage II and III at 550 °C. No post-deposition treatments were performed. The 70 nm CdS was deposited by 6-min chemical bath deposition at 65 °C, using the precursors thiourea and $CdSO_4$, and NH_3 as a complexing agent.

A 500 nm thick i-ZnO layer was deposited using room temperature RF sputtering. The substrates were mounted on a moving carrier that passes by a rectangular sputtering target at 7 cm/min such that during a single pass about 50 nm of i-ZnO is deposited. For a 500 nm thick i-ZnO, 10 consecutive passes of the carrier were carried out.

2.2. Polishing

The half fabricate (glass/Mo/CIGS/CdS/i-ZnO) with (natural) rough surface morphology was cut in samples with a size of 2.5 × 2.5 cm. The samples were mechanically polished using non-dry polishing fluid and a 200 mm diameter chempolishing pad. The rotational speed both the mounting head and the table was set to 150 RPM, rotating in opposite directions. The applied downward forces were set to 10 N or 20 N, resulting in 16 kPa and 32 kPa pressure, respectively. Using these two pressures, polishing times were varied. After polishing, the slurry was removed from the surface by scrubbing with acetone and DI-water. These smoothened half fabricates have been characterized with an atomic force microscope and inspected with cross sectional scanning electron microscopy (SEM).

2.3. Fabrication of the top sub-cell

The top subcells were fabricated in a PE-CVD cluster tool having dedicated chambers for layers with different types of doping. Firstly, a 30 nm of phosphorus doped hydrogenated nanocrystalline SiOx:H (*p*-nc-SiO_x:H) was deposited. This was followed by two nanocrystalline SiOx: H, layers of 7 nm and 14 nm in thickness with different doping concentrations. The first *p*-nc-SiO_x:H layer (with a narrower bandgap) serves as part of the tunnel recombination junction. The following layer was a wider bandgap p-layer to serve as hole-collector in the top sub-cell. After deposition of the amorphous silicon, another 30 nm n-type nanocrystalline *n*-nc-SiO_x:H was deposited, and the cell is completed by RF sputtering an ZnO:Al 250 nm front electrode. As a final step, a 300 nm Ag front grid was evaporated on the devices. The short circuit current of these devices was determined with by EQE, and V_{oc} and *FF* with a triple A rated *JV* tester, calibrated with calibration diodes from the Fraunhofer ISE institute.

2.4. Texturing of the front electrode

In this work, the ZnO:Al front electrode has been wet-etched to create a front texturing. Regarding the experimental design, it is crucial that there is a full area coverage of ZnO:Al, as the 250 nm of ZnO:Al (after etching) serves as a protective layer, preventing any water and acid ingression to the cells underneath. The deposition pressures have been varied between 1.5 μbar, 2.5 μbar, and 3.5 μbar and deposition temperatures between 100 °C, 125 °C, and 150 °C. Higher temperatures are unsuitable in this architecture, considering that ZnO:Al is the final layer to be processed in these devices and higher temperatures would induce undesired diffusion of cadmium. In all cases etching was done in a 0.5% HCl bath for 45 s. After etching, the sample was rinsed for at least 3 min in DI water. The initially deposited thicknesses of ZnO:Al were optimized as such that a 250 nm layer of textured ZnO:Al remained after etching. As the etching rate was dependent on the deposition parameters, the initial thicknesses of the ZnO:Al was varied.

3. Results

3.1. Polishing

The deposition of the 500 nm i-ZnO layer was performed in 10 consecutive passes of the carrier by the sputtering target. This