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Charge carrier transport mechanisms of passivating contacts studied by temperature-dependent J-V measurements

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ABSTRACT

The charge carrier transport mechanism of passivating contacts which feature an ultra-thin oxide layer is investigated by studying temperature-dependent current-voltage characteristics. 4-Terminal dark *J-V* measurements at low temperatures reveal non-linear *J-V* characteristics of passivating contacts with a homogeneously grown silicon oxide, which result in an exponential increase in contact resistance towards lower temperature. The attempt to describe the *R(T)* characteristic solely by thermionic emission of charge carriers across an energy barrier leads to a significant underestimation of the resistance by several orders of magnitude. However, the data can be described properly with the metal-insulator-semiconductor (MIS) theory if tunneling of charge carriers through the silicon oxide layer is taken into account. Furthermore, temperature-dependent light *J-V* characteristics of solar cells featuring passivating contacts at the rear revealed a FF drop at $T < 205$ K, which is near the onset temperature of the exponential increase in contact resistivity.

1. Introduction

Passivating and carrier-selective contacts based on a thin silicon oxide layer and a heavily-doped Si layer (poly-Si or Si-rich SiC_x) have recently attracted attention for their low recombination current densities < 10 fA/cm^2 while maintaining contact resistivities sufficiently low for solar cell contacts [1–10]. Although solar cells with efficiencies above 25% have been realized [11], the underlying physical transport mechanism of these contacts is still not fully understood. In general, it should be noted that although the principal structure of the above-mentioned contacts is similar, the process steps differ quite significantly, especially the thickness of the oxide and the final thermal treatment which makes it difficult to generalize theories about the underlying physical transport mechanisms.

Soon after the advent of the poly-Si emitter for bipolar junction transistors (BJTs) in the 1970s, different models were proposed to explain the current gain enhancement by the poly-Si emitter. An excellent review paper can be found here [12]. Among those, the most famous was the “oxide tunneling” model which described very adequately the reduction of the base current and the increase of the emitter resistance of BJTs with deliberately grown interfacial oxide [13]. For the hole current of n^+-poly-Si/c-Si(p) junction it reads:

$$J_p \approx q\sqrt{\frac{k_B T}{2\pi m_h^*}}\frac{P_t}{N_{D,int}} n_{i,int}^2 \exp\left(\frac{q}{k_B T}(V_j - \phi_s)\right). \quad (1)$$

In this expression $N_{D,int}$ and $n_{i,int}^2$ are the donor concentration and the intrinsic carrier concentration at the interface, respectively, V_j is the internal junction voltage, and ϕ_s is the surface band bending in the c-Si. The tunneling probability, P_t, is solved with the Wentzel-Kramers-Brillouin (WKB) approximation

$$P_t \approx \exp\left(-\frac{2}{\hbar} t_{ox}\sqrt{2m_h^* q\Delta\phi_h}\right). \quad (2)$$

According to Eq. (2), the tunneling probability decreases exponentially with the oxide thickness, t_{ox}, and the height, $\Delta\phi_h$, of the energy barrier. As one can readily see Eq. (2) is of the same form as the equation for the direct tunnel current in a metal-oxide-semiconductor (MOS) system, with the heavily-doped poly-Si showing metal-like behavior (degenerate doping). The assumption that tunneling is the dominant transport mechanism was further substantiated by the weak temperature dependence of these devices [12]. However, the model does not describe pnp BJTs well. In essence, the oxide poses a larger

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barrier to holes than to electrons which is reflected in the barrier heights $\Delta\phi_h = 1.0$ eV and $\Delta\phi_e = 0.3$eV determined with this model [12]. However, in the case of a pnp transistor this means that a slight current gain enhancement would come at the expense of a very high emitter resistance which does not reflect the experimental findings [14–16]. In addition, it should be noted that the reported values for $\Delta\phi_e$ and $\Delta\phi_h$ are much lower than the conduction (3.2 eV) and valence (4.7 eV) band offsets between c-Si and bulk SiO_2 [17]. Apart from tunneling over the oxide barrier, transport could also be realized through pinholes in the oxide, which are reported to be formed under certain experimental conditions. In view of the approach by Gan and Swanson [18] which capitalizes on deliberately formed pinholes in a thick oxide ($t_{ox} \geq 2$ nm), a model accounting only for transport through pinholes was recently published [19,20]. Furthermore, a technique not only capable of visualizing pinholes but also capable of quantifying the pinhole density has been published [21]. Yet it is still to be demonstrated that moderate annealing conditions ($T_{anneal} < 900$ °C) lead to a significant pinhole density. In addition, the pinhole model does not explain the *J-V* characteristics of non-annealed poly-Si/SiO_x/c-Si structures, which also yielded significant current gain enhancement factors [22].

In this manuscript, the transport mechanism is studied in detail by means of temperature dependent *J-V* measurements on test structures and solar cells. We compare three different TOPCon structures where oxide integrity ranges from fully intact to strongly disintegrated and show that their distinct *J-V* temperature-dependence can be explained with their structural differences. The TOPCon structure features an ultrathin oxide ($t_{ox} \approx$ 1.2–1.4 nm) which should suffice the requirements for an efficient carrier flow via quantum mechanical tunneling [23].

2. Experimental details

2.1. Sample preparation

A range of TOPCon structures with varying oxide integrity and thus electronic quality with respect to surface passivation and contact resistivity was prepared. Both symmetric lifetime samples and unipolar test structures featuring an ohmic rear contact and a circular metal contact on the TOPCon structure at the front (c.f. Fig. 1) were realized on shiny-etched (100)-oriented, 200 µm thick, 1 Ω cm n-type wafers. The TOPCon structures were realized by growing a thin oxide in boiling nitric acid (68%), depositing 15 nm silicon-rich a-SiC_x:H(n) by PECVD, thermal annealing, and, finally, hydrogen passivation at 400 °C. Three different annealing conditions were chosen: (i) 800 °C, 60 min; (ii) 900 °C, 10 min; and (iii) 950 °C, 3 min. At $T_{anneal} = 800$ °C the a-SiC_x layer remains amorphous, while it becomes partially crystalline for $T_{anneal} \geq 900$ °C as evidenced by Raman spectroscopy shown in Ref. [4].

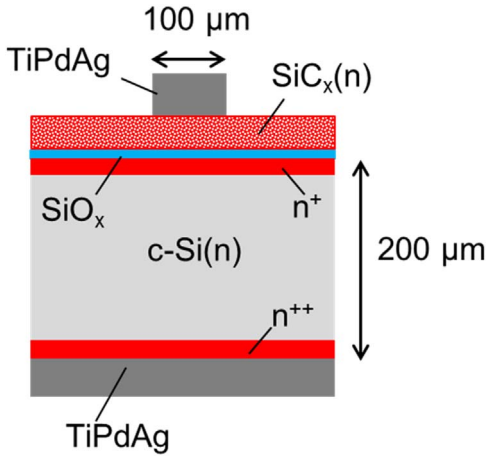

Fig. 1. Sketch of the unipolar test structure.

The unipolar test structures received a full-area metal contact at the rear and circular metal contacts with radius of ~ 53 µm (determined by optical microscopy) at the front as shown in Fig. 1. Metal was deposited by thermal evaporation of Ti, Pd, Ag. The electrodes were structured by the lift-off technique. The rear was fully metallized by thermal evaporation of Ti, Pd, Ag.

Solar cells featuring a boron-diffused emitter at the front and an n-type TOPCon contact at the rear were realized as described in Ref. [24]. The TOPCon structure was annealed at 800 °C, 60 min, and 900 °C, 10 min, respectively.

2.2. Characterization

The test structures were mounted onto a gold ceramic and the front electrode was contacted to a conductive pad by a bonded gold wire. The ceramic was then mounted into a cooling system and two probes made contact to the front pad and two contacted the chuck. The sample under investigation was cooled down to a temperature of about 114 K by liquid nitrogen. Before each *J-V* curve acquisition, the temperature was held for 2 min to establish thermal equilibrium. *J-V* data were taken in a temperature range of 114–350 K.

Temperature-dependent *J-V* data of the solar cells were taken by using a home-built hybrid light-emitting diode halogen lamp solar simulator with a temperature controllable chuck. More information on this setup can be found in Ref. [25].

3. Experimental results

3.1. Surface passivation and contact resistivity

The implied V_{oc} and contact resistivity (ρ_c) of the different TOPCon structures are displayed in Table 1. It can be seen that both the highest iV_{oc} and ρ_c were obtained for $T_{anneal} = 800$ °C. With increasing T_{anneal} both iV_{oc} and ρ_c decreased. At 950 °C virtually no surface passivation was obtained which can be ascribed to a complete disintegration of the tunnel oxide. In Fig. 2a TEM micrograph shows that for this annealing condition the oxide is completely "balled up", which leads to epitaxial regrowth of the Si layer on the c-Si wafer. Furthermore, diffusion of phosphorus from the SiC_x layer into c-Si is enhanced with temperature and instead of a very shallow diffused c-Si region (depth < 50 nm for $T_{anneal} = 800$ °C) a few 100 nm deep c-Si(n^+)-layer was formed which had a sheet resistance of about 850 ± 100 Ω/sq and 194 ± 5 Ω/sq in the case of 900 °C and 950 °C, respectively.

3.2. Dark J-V on test structures

The unipolar test structures featuring TOPCon at the front were measured in a temperature range from 114K to 350 K. Fig. 3a) shows the dark *J-V* characteristics of the sample structure featuring n-TOPCon annealed at 800 °C. At $T = 114$ K a non-linear *J-V* characteristic was observed showing a symmetric shape with respect to voltage. With increasing temperature, the current increased and at $T = 243$ K the *J-V* characteristic exhibited an almost linear shape. The latter denotes a transition from a Schottky contact to an ohmic contact. Fig. 3b) shows the *J-V* curves of the sample which was annealed at 900 °C. In the

Table 1
Sample description.

T_{anneal}	Oxide integrity[a]	iV_{oc} (mV)	ρ_c [mΩ cm^2]
800 °C	High	715.5	3.9 ± 0.4
900 °C	Medium	683.3	1.7 ± 0.3
950 °C	Low, many pinholes	624.7	0.5 ± 0.1

[a] Qualitative figure of merit.