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Band alignment of front contact layers for high-efficiency CdTe solar cells

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ABSTRACT

Resistive oxide materials play an important role in the front contact of CdTe solar cells. The high-resistance transparent (HRT) or "buffer" layer has been used extensively in CdTe thin-film photovoltaics to enable a reduction in CdS thickness while maintaining near-maximum device voltage and fill factor. SnO_2- and ZnO-based alloys were tested as HRT layers on a fluorine-doped tin oxide transparent conducting oxide. SnO_2-based alloy HRT layers were deposited via atmospheric pressure chemical vapor deposition (APCVD). Alloying ZnO with MgO to create $Mg_xZn_{1-x}O$ (MZO) via radio-frequency sputter deposition was explored as a way to reduce the electron affinity of ZnO HRT layers. To fully understand the behavior of these materials, many devices were fabricated with either no CdS layer, a sublimated CdS layer, or a sputtered, oxygenated CdS layer. MZO layers resulted in high open-circuit voltage and device efficiency even with the complete elimination of the CdS layer. In both HRT systems, controlling electron affinity to optimize front contact band alignment is an important consideration. Band measurements using photoelectron spectroscopy and synchrotron techniques correlate band alignment measurements with efficiency parameters in the design of HRT and CdS layers.

1. Introduction

Cadmium telluride thin-film solar cells have recently seen a rapid increase in record cell efficiency to 21.5% [1]. Part of this increase is due to the high optical collection of this technology [2]. Typically, CdTe thin-film solar cells are grown in the superstrate configuration, using glass coated with a transparent conducting oxide (TCO). Another oxide layer, dubbed the high-resistance transparent (HRT) or "buffer" layer, is often deposited on the TCO. "High-resistance" does not necessarily mean insulating but orders of magnitude more resistive than the TCO. Typically, a CdS-based layer is deposited on the HRT. CdS is a strong absorber of light with energy above its bandgap of 2.4 eV, and light absorbed in this layer is wasted because carriers photogenerated in the CdS are not collected. When the CdS layer is too thin the operating voltage of the cell degrades, so the CdS thickness that optimizes efficiency must balance current and voltage at the maximum power point.

Empirically, the presence of an HRT layer has been shown to lessen the degradation in voltage as the CdS thickness is decreased, allowing a thinner CdS layer and higher optimum efficiency. While the resistance of the layer plays a role in its effect, not all resistive oxides are effective HRT layers, and other electronic properties must also be considered. A recent review by Klein explains the science of interface band alignment in chalcogenide semiconductors and discusses the CdS/CdTe interface as well as different oxides used as HRT layers [3]. In previous work by the authors, a highly transparent oxygenated CdS layer was shown to be compatible with one SnO_2-based HRT and the importance of band alignment for the oxygenated CdS layer was shown [4]. Here, a combination of numerous device results, modeling, and band measurements show the importance of band alignment using HRT layers within the zinc oxide and tin oxide systems. Cells are demonstrated using oxide layers that allow for high efficiency with the elimination of the CdS layer.

The most commonly used TCO in commercial CdTe cells is fluorine-doped SnO_2 (FTO) because it can be deposited during the glass manufacturing process with high throughput and is mostly inert to subsequent processing steps. Still, cells have successfully been made using In_2O_3:Sn [5], Cd_2SnO_4 [6], and ZnO:Al [7]. Many TCO/HRT combinations have been studied, with HRT layers including ZnO [8], In_2O_3 [9,10], Ga_2O_3 [9], SnO_2 [11,9,10,12], and alloys of these materials such as zinc stannate [13,14]. A universally described feature of these layers is their increased resistivity relative to the TCO.

One hypothesis of the HRT's role in CdTe solar cells considers

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the effect of pinholes, or small areas where there is no CdS coverage, and through which CdTe directly contacts the oxide layer. According to this explanation, a diode with maximum open-circuit voltage and fill factor will be formed regardless of layer thickness as long as there are no CdS pinholes. The pinhole area that contacts the oxide below is a weaker diode with high forward current and low open-circuit voltage [9]. A loss in open-circuit voltage occurs when CdS thickness is reduced, and this is ascribed to an increasing fractional pinhole area the substrate [12]. This theory assumes that pinhole area increases as overall CdS layer thickness decreases. By adding an ohmic resistor between the TCO and the CdS, the theory states, less CdS is required because the shunting effect of the pinhole area is reduced.

In devices made at Colorado State University there is no evidence that the existence of pinholes is correlated with CdS layer thickness [15]. Electron microscopy has shown that films 20–30 nm thick have coalesced grains without exposing the TCO. Thicknesses of close to 100 nm of this CdS material are needed to obtain maximum open-circuit voltage. Statistical measurements have not shown an increase in pinhole area with reduced CdS thickness for films made at CSU . Devices that have both lower pinhole area and reduced CdS thickness nevertheless show lower V_{OC} relative to a control, indicating that CdS layer thickness is an important variable independent of pinholes [16]. Overall, the role of the HRT has not been considered clear or fully understood with yet another possibility involving the effects of thermal expansion [17]. Further understanding of which material properties affect HRT function is needed to find more ideal contacts which allow the most light possible to reach the absorber. Here, band alignment of the front contact layers, which is known to be important but seldom discussed in this context, is investigated as a key concept to complement the existing understanding.

2. Material and methods

All devices reported in this work fall within the following structure: the glass is 3.2-mm soda-lime glass, the TCO is fluorine-doped tin oxide, the HRT is either absent, SnO_2-based, or ZnO-based, and the CdS layer is either absent, sputtered oxygenated CdS, or sublimated CdS. Commercial low-iron soda-lime glass coated with 10-$\Omega/\square$ SnO_2:F TCO ("R10H1" manufactured by PPG Industries, Inc.) was the baseline substrate for the SnO_2-based HRT layers studied here. SnO_2-based HRT layers were deposited on FTO using atmospheric pressure chemical vapor deposition (APCVD) in a laboratory reactor, which simulates the in-line manufacturing process. All SnO_2-based HRT layers deposited by PPG Industries had tin as a minimum of 80 at% of cations. Radio-frequency sputter-deposited ZnO-based layers were deposited on TEC 10 (manufactured by Nippon Sheet Glass Co., Ltd.), a similar FTO-coated soda-lime glass product. For these layers a 10-cm diameter target was used with a power of 180 W, frequency of 13.56 MHz, a pressure of 5 mTorr, 1% O_2 in argon, and a target-substrate distance of 15 cm. Targets were 99.99% pure, hot-pressed, mixed-powder targets (Plasmaterials, Inc.) with a 99.999% pure ZnO target (Kurt J. Lesker) used for comparison.

Complete thin-film CdTe solar cells were prepared in the CSU Advanced Research Deposition System (ARDS). This system was used for sublimated CdS, CdTe, $CdCl_2$ and Cu process steps. Cell fabrication and oxygenated CdS procedures have been described in detail [4]. Solar cell efficiency measurements were performed using a xenon arc lamp with AM1.5 filter; short-circuit current density was calibrated to cells measured by NREL.

Band measurements were performed using a PHI 5800 X-ray Photoelectron Spectroscopy system with a PREVAC UVS40A2 UV source. Samples were cleaned and heated in the ARDS to approximate the condition of the surface prior to semiconductor deposition, removed from the ARDS under an inert environment, and prepared in a glovebox under argon. Air exposure of the samples was less than 10 s during loading into the XPS system to limit atmospheric contamination of the surface. Measurements had a take-off angle of 85° and a sample bias of −5 V. Analysis followed the procedure of Helander et al. [18]. Synchrotron-based measurements were performed on beamline X1B at the National Synchrotron Light Source at Brookhaven National Laboratory. A beam energy of 550 eV was used for XES which corresponds to an attenuation length in SnO_2 of 80 nm [19]. A range of approximately 522–554 eV was scanned to obtain the O-K-edge XAS.

3. Results

3.1. SnO_2-based HRT layers

Many candidate SnO_2-based HRT layers were tested in devices with various alloying elements, alloy compositions, and thicknesses. Alloying elements tested were Zn, Ga, In, and N as well as un-alloyed tin oxide in the thickness range of 80–250 nm. These layers were screened to test quickly which were most effective. A preliminary experiment was devised with one substrate each of thick (>120 nm) and thin (<90 nm) sublimated CdS using both the TCO/HRT/CdS/CdTe and TCO/CdS/CdTe structures. The difference between voltage and fill factor of these devices with and without HRT was statistically tested to determine if an HRT effect was significant. The best-performing SnO_2-based HRT layer was found to be a dilute (2–3 at%) zinc-doped tin oxide using monobutyl tin trichloride and diethyl zinc as precursors; an HRT thickness of 150 nm was found to be optimal. This HRT layer was used in subsequent experiments in which the sublimated CdS layer thickness was varied.

Devices with the structure TCO/HRT/sublimated CdS/CdTe were made using the SnO_2:Zn HRT, and devices with the structure TCO/sublimated CdS/CdTe served as a control (see Fig. 1). Device quality had little dependence on CdS layer thickness above a critical value of about 90 nm for devices without HRT and 60 nm for devices with HRT. Below this value, V_{OC} gradually declined with a minimum at 0 nm (a device with no CdS layer). Meanwhile, current continuously improved with thinner CdS. Devices with the HRT showed both a lower critical thickness and a higher V_{OC} with 0 nm of CdS. For all values of CdS thickness, devices typically exhibited high shunt resistance. The best devices with the structures TCO/CdTe, TCO/HRT/CdTe, TCO/CdS/CdTe, and TCO/HRT/CdS/CdTe are shown in Fig. 2. With a CdS layer, the increased current with HRT was a greater effect than the slightly reduced voltage, highlighting the importance of short-circuit current gains as the benefit of the HRT layer.

CdTe devices often show light-dark crossover that increases as CdS thickness decreases. Some devices with the structure TCO/CdTe (without any HRT or CdS layer) exhibit strong light-dark crossover, in which even low illumination levels cause a large drop in series resistance compared to the dark measurement. This behavior was examined by illuminating the devices with red and blue light-emitting diodes and varying the supply current by several orders of magnitude; both the LED current and the short-circuit current were measured, and remained linearly related over the measurement range. Fig. 3a illustrates the drastic change in series resistance as LED intensity is varied over several orders of magnitude, corresponding with a change in photocurrent. Fig. 3b illustrates this phenomenon in parametric form for both blue and red LED illumination. The relationship between J_{SC} and series resistance for this device is comparable when red and blue LEDs are used. The presence of light greatly reduces the barrier to forward