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Low-defect metamorphic Si (Ge) epilayers on Si (001) with a buried template of nanocavities for multiple-junction solar cells

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ABSTRACT

Si (001)-oriented substrates (p-type) were implanted at 10 keV with He^+ ion doses in the 5×10^{15} cm^{-2} range. They were annealed at 973 K for 1 h to create a buried layer of nano-sized bubbles. Layers of $Si_{0.77}Ge_{0.23}$ about 215 nm thick were grown by low pressure chemical vapor deposition at 848 K on these silicon wafers. The surface roughness and morphology were checked by atomic force microscopy and optical microscopy before and after etching with a modified Shimmel recipe to reveal etch pit dislocations. The thickness, composition, crystalline quality and relaxation-state of the SiGe layer were assessed by Rutherford backscattering spectroscopy and high-resolution X-ray diffraction. A fully relaxed strain-state was obtained for $Si_{0.77}Ge_{0.23}$ layers that did not exhibit the classical cross-hatched pattern morphology while having a threading-dislocations density below 10^3 cm^{-2}. This low dislocation density was confirmed by photoluminescence spectroscopy. From high resolution transmission electron microscopy observations, the quasi-total strain-relief is assumed to take place by emission of dislocation loops protruding down into the Si substrate from the SiGe/Si interface and terminating at void surfaces of the buried-nanoporous layer. Possible annihilation of dislocation segments coming from either the SiGe/Si interface or punched out in glide planes by overpressurized nanobubbles may also occur. This near surface porous Si is well adapted for multiple junction solar cell manufacturing.

1. Introduction

Light emitted by the sun and falling on Earth is one of the most plentiful energy resources on the planet. Over 1.5×10^{22} J (1.5×10^4 EJ) of solar energy reaches Earth every day, compared to a daily energy consumption of approximately 1.3 EJ by human activity [1]. However, solar radiation is a broadly distributed energy resource both in terms of geographic distance, requiring large, expensive collectors, and in terms of its wide range of wavelengths. Since three decades, there are continuous efforts to find ways to decrease the cost-effectiveness ratio of solar cells. With regard to efficiency only, multiple junction solar cells (MJSCs) are a well-known technology based on layering of different p/n junctions formed by semiconductors of increasing band-gaps, from the lowest band-gap bottom cell to the topmost cell having the shortest absorption wavelength. To avoid photo-voltage drop, p^+/n^+ tunnel junctions are used to provide a low electrical resistance and optically low-loss connection between two sub-cells. This allows the best match to the solar spectrum and photo-carriers collection; theoretical limits of efficiency being 34/37% (Shockley–Queisser) [2,3], 42/55%, 49/63%, 53/68%, and 68/86% for 1, 2, 3, 4 and infinite number of p/n junctions in un-concentrated sunlight or full 46,000 × suns concentration, respectively. A road-map based on the number of junctions quickly clashes with the cost and complexity increase of these epitaxial stacks, as the number of junctions needed to get equal efficiency increments increases exponentially. In order to cover the infrared part of solar spectrum with a bottom cell (for getting a higher open-circuit voltage V_{OC}) and to reduce the defect density (hence the dark current), lattice-matched (LM) preferably to metamorphic (MM) epitaxial stacks were fabricated historically on GaAs, Ge and InP and even on GaSb substrates.

The counterpart of such a strategy is the increased cost of the III–V substrate. The 2013 record efficiencies were 28.8% (1J, Alta Devices), 31.1%/34.1% $^{467\times}$ (2J, LM, NRE), 37.9%/44.4% $^{302\times}$ (3J, IMM, Sharp), 43.5% $^{418\times}$/44% $^{947\times}$ (3J, LM, Solar Junction), 43.6% $^{319\times}$ (4J, MM, Wafer Bounding, Soitec et al.), and 38.8% (5J, Boeing Spectrolab). Hence Ge appears to be the substrate of choice, particularly for those LM-InGaP/(In)GaAs/Ge MJSCs designed with additional GaInAsNSb junction between (In)GaAs and Ge for better current match.

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Numerous architectures of lattice-relaxed Ge (Si) pseudo-substrates (PSs) on Si(001) have been developed earlier for strained SiGe CMOS (complementary metal oxide semiconductor) technology [4]. However these methods have been supplanted by (expensive) SOI and GeOI (silicon or germanium on insulator) [5] wafers, which allows the electrical insulation of CMOS devices. Owing to the lattice mismatch between Si and Ge of 4.2%, strain is unavoidably introduced in epitaxial SiGe layers grown on Si. The strain will be either stored as strain energy in the film or accommodated by a network of misfit dislocations at the interface [6,7]. Unfortunately, these misfit dislocations are accompanied by a high density of threading dislocations ($>10^9\,cm^{-2}$) [8] which extend to the surface of the SiGe and are unacceptable for optoelectronic and microelectronic devices.

In this context, many approaches were explored to tackle this problem of manufacturing strain-relaxed SiGe/Si pseudo-substrates, having a high-structural quality in terms of relaxation rate, morphology and a defect density lower than $10^4\,cm^{-2}$. The first result was obtained by Fitzgerald et al. [9] and Bozzo et al. [10] with several microns thick compositionally linearly/graded SiGe buffer layers by molecular beam epitaxy (MBE) and chemical vapor deposition (CVD) respectively at relatively high temperature (greater than 873 K). It allowed misfit dislocations to propagate large distances, the dislocation nucleation being governed by the slow increase in strain induced by varying the Ge content (x) of the SiGe alloy. The second result was reported by Chen et al. [11] making use of a Si buffer layer grown at a low temperature (LT, 723 K) by molecular beam epitaxy (MBE) [12]. In this method, point defects, which are introduced in the Si buffer layer grown at low temperature, enhance the nucleation and multiplication of dislocations and relieve the strain in the overgrown SiGe film [13,14]. A disadvantage of the LT methods is, however, that the growth is not feasible in gas source systems such as chemical vapor deposition (CVD) and gas source MBE, since growth temperature higher than 400 °C is necessary for decomposition of gas sources. In all results, the reported threading dislocations density in the SiGe buffer layer varied between $10^4\,cm^{-2}$ and $10^9\,cm^{-2}$ which is unacceptable for their use either in microelectronic or optoelectronic devices.

However, 10 years ago, a new approach discovered by several groups [15,16] allowed for high degrees of relaxation and low threading dislocation densities to be produced. It consisted of an implantation (after or during the growth of SiGe) by He^+ or H^+ followed by thermal annealing [17–21]. The latest was of major interest for the next generation of high compatible devices like CMOS output. It was based on the concern of preserving the SiGe pseudo-substrates from the possible implantation damage. However, the easiest way was to schedule the implantation before the SiGe growth step, after some upstream trials with different noble gas and implantation conditions [21–24]. Depending on the latter, various types of He bubbles connected with different dislocation reactions were observed [25]. The interaction between bubbles and dislocations requires the bubble layer to be separated from the interfacial region [26,27].

In this work a straightforward method is proposed to grow a fully-relaxed low-defect SiGe layer on Si (001) by coupling He^+ implantation and LP-CVD mode. This approach produces high quality threading dislocation density (lower than $10^3\,cm^{-2}$), thin relaxed SiGe layer ($\approx(210\pm5)$nm) and smoothed SiGe surface. The relaxation mechanism of $Si_{0.77}Ge_{0.23}$ layers was studied on Si substrates implanted by He^+ and annealed. The roles of the nanocavity layer for blocking of the dislocation loop expansion are discussed using transmission electron microscopy (TEM) observations, high resolution X-ray diffraction (XRD), Rutherford back scattering spectroscopy and photoluminescence (PL) measurements.

2. Experiment

2.1. Nanocavity layer formation

Stopping and range of ions in matter (SRIM) simulations were used to determine He profiles to pick up the most pertinent implantation parameters [28]; (001) p-type Si wafers were implanted at room temperature with He^+ at 10 keV, with a flux of about $(9.0\pm0.3)10^{12}\,cm^{-2}\,s^{-1}$ at high fluences ($5\times10^{15}\,cm^{-2}$) to address the role of the porous layer (position from the surface and porosity) on the relaxation mechanism. The latter was chosen thanks to Monte Carlo simulations giving a He projection range R_p of (110 ± 50) nm. The sample was annealed in the CVD reactor at 973 K for 1 h to check the thermal stability of the nanocavities [4]. A Si substrate having undergone such process, thus containing a buried porous zone near the surface will be called Si template.

2.2. Epitaxial and characterization of SiGe layer

After a chemical cleaning step of the Si template by using a Shiraki process [29], SiGe growth was carried out by LP-CVD mode at 823 K for 15 min using a gas ratio of SiH_4 (60%):GeH_4 (37%) at a working pressure of 2.4×10^{-2} Torr. The SiGe PSs thickness was determined both from HR-TEM measurements in cross section view and from the simulations of the RBS spectrum obtained in random channeling conditions. The dislocation density was estimated by HR-TEM and by dislocation etch pit counts both on optical and atomic force microscope images, after using the Shimmel solution composed of CrO_3 (0.3 M) and HF (50% in de-ionized water). For better statistics, some panoramas were carried out on the SiGe surfaces. The crystalline quality was checked both by HR-TEM and RBS in channeling mode. The state of relaxation (R) and Ge composition were derived from the well-known method based on high resolution X-ray diffraction (HR-XRD) in symmetric and asymmetric configurations [30]. The Ge compositions were compared to those obtained by RBS using the ratio of integrated intensities of Si and Ge peaks. The NP-TO peaks, famous dislocation series (D1–D4) in the SiGe PS were revealed by optical technique using a 514 nm Ar^+ laser (with lightening power of 200 mW) and sample temperature of 8.3–12.5 K.

3. Results and discussion

3.1. Characterizations of the manufactured SiGe PS

The SiGe PSs strain relaxation strongly depends on the localization of the voids generated by He^+ implantation and by annealing which was optimized by several groups [25,31–34]. However, if the He^+ projected range is near the SiGe/Si interface, voids nucleate there, resulting in a high surface roughness and threading dislocation density. The interaction between bubbles and dislocations requires the bubble layer to be separated from the interfacial region [26,31–36]. The location of voids emerges as one of the key points to exploit He^+ implantation for $Si_{1-x}Ge_x$ relaxation.

Fig. 1a displays the AFM image of the surface roughness of the SiGe PS, which has an RMS of 4 nm over 40 μm × 40 μm. In this image the absence of cross-hatched pattern (misfit dislocations) was obvious. Actually, it is observed in the non-implanted SiGe/Si presented in Fig. 1b [28], in which the threading dislocation density can be estimated, with low statistics, at $5\times10^5\,cm^{-2}$. After chemical etching, dislocation etch pits are revealed in Fig. 2a and demonstrate that the dislocation density is lower than $10^3\,cm^{-2}$ in $Si_{0.77}Ge_{0.23}$ grown on He-implanted Si (001). This optical image shows the absence of any cross hatched pattern which is casually

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