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Experimental demonstration of the effect of field damping layers in quantum-dot intermediate band solar cells

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ABSTRACT

Intermediate band solar cells must demonstrate the principle of voltage preservation in order to achieve high conversion efficiencies. Tunnel escape of carriers has proved deleterious for this purpose in quantum dot intermediate band solar cells. In previous works, thick spacers between quantum dot layers were demonstrated as a means of reducing tunnel escape, but this approach is unrealistic if a large number of quantum dot layers have to be grown. In this work we report experimental proof that the use of field damping layers is equally effective at reducing tunnel carrier escape, by reducing the potential drop in the QD-stack and the associated electric field. Moreover, we demonstrate that the fact that tunnel carrier escape takes place under short-circuit conditions does not imply that voltage preservation cannot be achieved. We describe a theory that relates the evolution of the tunnel escape to bias voltage and the preservation of the voltage in an IBSC. Temperature and voltage-dependent quantum efficiency measurements, temperature dependent open-circuit voltage measurements and calculations of the internal electric field in IBSCs serve as the basis of the proposed theory.

1. Introduction

Intermediate band solar cells (IBSCs) [1] must fulfill the *voltage preservation* principle in order to achieve high conversion efficiencies. This principle states that the output voltage of such a solar cell is only fundamentally limited by the bandgap, E_G, of the intermediate band (IB) host material. The two additional sub-bandgaps resulting from the presence of the IB – E_H for the larger and E_L for the smaller – contribute to an increase of the photocurrent of the solar cell but do not set a limit to the operation voltage. Three quasi-Fermi levels (QFLs) are needed to describe the electronic population of the three bands of an IBSC working in accordance to the voltage preservation principle: ε_{Fe}, ε_{FIB} and ε_{Fh}, for the conduction band (CB), IB and valence band (VB), respectively [2]. The voltage preservation principle has been verified so far in IBSC prototypes using InAs/GaAs quantum dots (QD) [3,4] or Ti-doped GaAs [5] as the IB material. The demonstration consists in measuring a photo-voltage larger than E_H/e and, in the limit, close to E_G/e, where e is the electronic charge. In all cases this has only been possible at low temperatures, because of the existence of a fast thermal escape of carriers from the IB to the CB at room temperature (RT) [6], which prevents the QFL split between these two bands.

For QD-IBSC prototypes, it has been demonstrated that tunnel-assisted carrier escape between the IB and the CB must also be eliminated for achieving voltage preservation [3,6]. Tunnel carrier escape is activated by the electric field that exists in the QD-stack, generally placed between p-doped and n-doped emitters. Electron tunneling between the IB and the CB can be avoided by growing thick spacers between two consecutive QD-layers [6]. This approach is not, however, without disadvantage. Thick spacers set a practical limit to the number of QD-layers that can be grown, by increasing both the time and the cost of each sample growth. A large number of QD-layers is desired to enhance sub-bandgap absorption, which is weak in current QD-IBSC prototypes [7]. The challenge remains in being able to fabricate IBSCs containing a large number of QD-layers and, at the same time, avoiding carrier tunnel escape. In Ref. [8] the use of field damping layers (FDLs) was proposed to sustain a large part of the potential drop between the emitters, so that the QD-stack is placed in a flat-band zone of the device. This approach aims to avoid tunneling between the IB and the CB (this will be discussed in detail later) without the need for increasing the thickness of the spacers between QD-layers, but no empirical evidence in this regard has yet been reported.

In this work we investigate experimentally the voltage preservation principle in three different QD-IBSC prototypes. For this, we analyze the temperature and voltage dependence of their quantum efficiency (QE), evaluating the impact of the spacer thickness and the

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FDLs. Finally we discuss how sub-bandgap QE, tunnel escape and voltage preservation are related.

2. Material and methods

2.1. Sample description

Three batches of samples, SC1, SC2 and SC3, were manufactured. SC1 coincides with S3 in Ref. [3] and with SB in Ref. [6]; the structure of SC2 is described in Ref. [8] and coincides with SC in Ref. [6] and S2 in Ref. [3]; and SC3 coincides with S1 in Ref. [3]. Detailed structures and growth conditions for these samples can be found in Refs. [3,6,8]. We indicate here the most relevant characteristic of these samples for the present work.

All samples contain a stack of InAs/GaAs QDs. Samples SC1 and SC3 correspond to a basic QD-IBSC layer structure: p-emitter/QD-stack/n-emitter. SC1 contains 30 layers of QDs, while SC3 contains only 10 layers. SC1 has thick (84 nm) spacers while SC3 has thin (10 nm) spacers. SC2 contains 10 layers of QDs separated by thin (13 nm) spacers. The key difference with respect to the other two samples is that the structure of SC2 includes two extra layers: a 100 nm thick layer of undoped GaAs between the n-doped emitter and the QD-stack, and a 170 nm thick layer of lightly doped n-GaAs between the QD-stack and the p-doped emitter. These layers perform as FDLs, sustaining most of the junction built-in potential, V_{bi}, so that QDs can be driven to a flat-band potential region under forward bias. These details, along with other, some of which will be introduced later, are summarized in Table 1. The simplified band diagrams under short-circuit conditions for each sample (SC1, SC2 and SC3, from left to right) are sketched in Fig. 1a. These sketches are intuitive graphical illustrations of the impact of both the spacer thickness and the FDLs in the band diagram of a QD-IBSC. They will serve also to define some parameters used in the discussion of our results. To preserve a common vertical scale, the band diagram of SC1, which is much thicker than the other two samples, is broken at some points. In Section 4 we will present calculation results of the actual band diagram in the QD regions of our samples.

2.2. Measurement conditions

Samples were mounted on a copper disk and placed in a closed-cycle He-cryostat. For the QE measurements, light from a halogen lamp was chopped and diffracted using a 1/4 m. monochromator. A low-noise amplifier was used both to amplify the photocurrent signal and to apply a bias voltage, V_{bias}, to the cells. V_{bias} is defined as positive when the amplifier positive terminal is connected to the p-side of the cell; i. e., we respect the sign criteria of the photo-induced voltage in a solar cell. The photocurrent detection was done using conventional lock-in techniques. For the measurement of the open-circuit voltage, V_{OC}, a He–Ne gas laser was used as a light source, providing an excitation power density of approximately one sun.

3. Results

Fig. 1b shows the measured Internal Quantum Efficiency (IQE) or External Quantum Efficiency (EQE) of the studied samples (SC1, SC2 and SC3, from left to right). Samples were measured at RT and at lower temperatures. The specific values of the temperature, T, are indicated in the figure. For each temperature, the QE was measured at different values of V_{bias}. The applied voltages, also indicated in the figure, range from 0 V to the maximum positive voltage that allowed for a tolerable noise in the measurement. Measurements are presented from 1.55 eV to lower photon energies in order to magnify the sub-bandgap part of the QE, which is more relevant in this work.

We will first briefly comment on the supra-bandgap QE. It decreases by around one order of magnitude for all samples at low temperature. We believe that the reason for the general decrease in EQE is due to non-ohmic or high-resistive behavior of the metal contacts at low temperatures. A reduction of V_{OC} must accompany the reduction in J_{SC}, however, for a particular value of T, the variation in V_{OC} for two different values of J_{SC}, J_{SC1} and J_{SC2}, is (assuming the superposition principle) equal to $\ln\left(J_{SC1}/J_{SC2}\right) \times mkT$, with $1 < m < 2$. A reduction of a factor 10 in J_{SC} would lead to a reduction of $m \times 21$ mV in V_{OC} for $T = 100$ K. Therefore, the small V_{OC} variations due to the decrease in EQE can be neglected in the forthcoming discussion on voltage preservation.

All samples exhibit non-zero sub-bandgap QE at RT. The energy of the lowest-energy peak of the QE is labeled E_H, as it corresponds to the larger of the two sub-bandgaps introduced by the IB. This energy is related to transitions from the ground state (GS) for holes to the GS for electrons in the QDs. E_{ES}, in turn, corresponds to the energy of the transition between confined first excited states (ES) for holes and electrons in the QDs. This is the transition configuration found theoretically [9] and experimentally [10] for InAs/GaAs QDs; for undetermined dot geometry the actual transitions could differ. For each

Table 1
Characteristic design features and measured and calculated parameters at $T = 10$ K, unless otherwise specified, of the studied samples.

Test sample	SC1	SC2	SC3
Number of QD layers	30	10	10
Si δ-doping level (cm^{-3})	3.4×10^{15}	1.9×10^{16}	3.6×10^{16}
p-emitter doping level (cm^{-3})	2×10^{18}	2×10^{18}	2×10^{18}
n-emitter doping level (cm^{-3})	1×10^{18}	2×10^{17}	2×10^{17}
d (nm)	84	13	10
W_{QD} (nm)	2655	160	110
FDLs	No	Yes	No
FDL n doping level (cm^{-3})	–	1×10^{16}	–
E_H (eV)	1.07[a]	1.03[a]	1.13
E_{ES} (eV)	1.14[a]	1.08[a]	1.21
E_G (eV)	1.52	1.52	1.52
V_{OC} (V) at RT	0.69	< 0.47	0.68
V_{OC} (V)	1.48	1.48	1.20
F_{max} (kV/cm) at $V_{bias} = 0$ V	−34.8	−47.5	−146.1
F_{max} (kV/cm) at $V_{bias} = E_H$/eV, assuming $V_2 = 0.2/0$ V	−14.6/−20.0	−4.0/−13.7	−60.2[b]
F_{max} (kV/cm) at $V_{bias} = E_{ES}$/eV, assuming $V_2 = 0.2/0$ V	−12.2/−18.3	−1.2/−11.4	−29.6/−53.1

[a] Extrapolated from values measured at higher temperatures.
[b] The use of V_2 does not hold in this case, since the whole QD-stack lies in the SCR.