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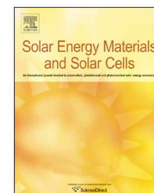

Lifetime assessment in crystalline silicon: From nanopatterned wafer to ultra-thin crystalline films for solar cells

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ABSTRACT

We have studied surface passivation on nanopatterned crystalline silicon (c-Si) wafers (280 μm), thin c-Si wafers (25 μm), ultrathin (∼1–6 μm) low temperature epitaxial PECVD and epitaxy-free silicon. Nanopatterned front surfaces were produced by combining nanoimprint lithography with dry or wet etching. The impact of the nanopatterning on the effective lifetime is investigated by means of photoconductance and time-resolved microwave conductivity measurements. Passivation of flat ultrathin monocrystalline layers by a-Si:H demonstrates effective lifetimes of a few μs. Flat, dry and wet etched c-Si wafers were also passivated by hydrogenated amorphous silicon, thus forming a heterojunction interface. The measured effective lifetimes were 2.2 ms for the flat, 484 μs for the dry and 709 μs for the wet etched wafers, respectively. It is noteworthy that despite the plasma damage associated with the dry etching process, the lifetime measured after passivation remains high enough for the targeted ultrathin solar cells. Solar cells fabricated on wafers nanopatterned via wet etching have reached an open circuit voltage as high as the flat sample thus demonstrating the potential of the use of wet etched nanopatterned surfaces for high efficiency solar cells.

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1. Introduction

In the field of crystalline silicon photovoltaics (PV), strong efforts are focused on reducing the wafer thickness, thus aiming at low-cost, lightweight and flexible cells. Solar cells with substantial material savings, via the reduction of the absorber thickness down to 40–50 μm and efficiencies above 20% have already been demonstrated [1]. Nowadays, devices with 10–20 μm thick absorbers have reached 15% efficiency [2], mainly limited by the reduced absorption in these thin layers. This limitation is even stronger for thinner solar cells (< 10 μm) [3,4]. To increase the absorption in ultrathin solar cells, various light trapping concepts can be implemented: antireflection coatings (ARC) [5], random pyramid texturing [6] and more recently, advanced nanophotonic concepts enabling the manipulation of light at the sub-wavelength scale [7–9]. The latter advanced light trapping shows a great promise for the use in solar cells with the potential to overcome the Lambertian light scattering limit [10]. This is due to the sophisticated engineering of the electromagnetic field distribution on the sub-wavelength scale combined with the optimization of the light propagation [11]. The main advantage of using nanopatterning is the small material waste (less than one micron) which is compatible with ultra-thin c-Si wafers.

The fabrication of nanopatterns generally involves two main processes: (1) defining the mask by lithography techniques, such as nanoimprint lithography (NIL) [12], laser interference lithography (LIL) [13] or hole–mask colloidal lithography (HCL) [14]; and (2) etching process for the formation of the pattern via reactive ion etching (RIE), inductively coupled plasma etching (ICP) or wet chemical etching using tetramethyl ammonium hydroxide (TMAH) and potassium hydroxide (KOH) [15]. These etching processes may result in surface damages and, as a consequence, the fabrication of these structures has to face a trade-off between the optimal optical and electrical properties in order to enable high efficiency solar cells [16–18]. Therefore, the development of an optimal surface passivation scheme (reducing the minority carrier recombination losses and maximizing the open-circuit voltage) is needed. Various materials based on amorphous silicon technology have been developed for the passivation of flat and textured wafers: hydrogenated amorphous silicon oxide (a-SiO_x:H) [19], hydrogenated amorphous silicon nitride (a-SiN_x:H) [20], and hydrogenated

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amorphous silicon carbide (a-SiC_x:H) stacks [19,20]. Yet, a thin hydrogenated amorphous silicon (a-Si:H) layer is able to passivate the surface silicon dangling bonds, resulting in high carrier lifetimes for both, textured and flat c-Si surfaces [21,22]. In this work we have used a-Si:H for the passivation of nanopatterned c-Si wafers (280 μm), thin c-Si wafers (25 μm) and an epifree film. Additionally, a low temperature PECVD epitaxial film has been dipped in hydrofluoric acid (HF) and the lifetime was measured. The photonic nanopatterns on c-Si wafers were fabricated by NIL technique and either dry or wet etching. The effective carrier lifetime was measured by photoconductance (PC) and time-resolved microwave conductivity (TRMC) setups. Finally, heterojunction solar cells with a thin intrinsic a-Si:H layer (HIT) were fabricated in order to identify the effect of the different etching processes on the electronic characteristics.

2. Characterization and fabrication methods

NIL is a direct mechanical lithographic technique which achieves nanopattern definition through the use of a hard mold with nanoscale surface-pattern. The mold is pressed into a surface polymeric film at optimal temperature and pressure. The pattern is stamped directly on the polymer material and the final definition of the pattern is transferred to the substrate by plasma etching. This technique is considered to be one of the most cost-effective producing nanopatterns with resolution down to 10 nm. The main limitations result from the physical nature of the contact, which reduces the efficiency on highly rough surfaces with defects or particles. Some of these considerations have been discussed in Ref. [12]. Two 280-μm thick p-type float zone (FZ) silicon wafers with a resistivity of 1–5 Ω cm and (1 0 0) orientation were used to test the nanopatterning process. On one of them we deposited a SiO_2 film on both sides as a hard mask to prevent uncontrolled etching during the wet chemical process. The nanopattern was formed by nanoimprint lithography using a polymer resist spin-coated directly on the c-Si surface (dry sample) or on the SiO_2 hard mask (wet sample) with a hexagonal array of holes. In the case of the wet sample, the pattern was transferred from the resist to the SiO_2 hard mask by CHF_3/O_2 plasma-etching and then the chemical etching of the c-Si surface was performed with 10% tetramethyl ammonium hydroxide (TMAH) diluted in water at 80 °C. The SiO_2 hard mask on the opposite side of the wafer prevented the random etching of the non-patterned surface. For the dry sample, the pattern was directly transferred to the c-Si surface from the NIL resist by reactive ion etching (RIE) using a SF_6/O_2 gas mixture at pressure of 100 mTorr. After the silicon etching, a sequence of H_2SO_4/H_2O_2 mixture (SPM) and hydrofluoric acid (HF) was used to remove the residual resist and the SiO_2 hard mask.

For passivation purposes, the native oxide was removed by 60 s long dipping in 5% diluted HF. Afterwards, a capacitively coupled RF (13.56 MHz) PECVD reactor has been used to deposit an a-SiC:H/a-Si:H stack at 200 °C from SiH_4 and CH_4 gas mixtures. The initial ultrathin a-SiC:H film (~1 nm) was used to prevent epitaxial growth on the (1 0 0) c-Si wafer. Finally, a 20 nm-thick a-Si:H film was grown from the dissociation of 50 sccm of silane at a pressure of 54 mTorr. Passivation on the ultrathin c-Si layer were performed in different technologies: (1) NIL-nanopatterned 280 μm c-Si wafers, (2) 4 in. DSP, 25 μm p-type CZ (1 0 0)-oriented wafer with a resistivity in the range of 1–20 Ω cm provided by University Wafer (USA), 3) a 6 μm-thick epitaxial film grown by PECVD at 175 °C [4] and (4) 1.1 μm (1 0 0)-oriented p-type epifree layer, obtained by reorganization upon annealing of cylindrical macropore arrays in silicon [10]. The epitaxial film was growth by PECVD at a substrate temperature of 175 °C on a (1 0 0) monocrystalline silicon wafer, the lift-off of the epitaxial layer from the wafer was done by a rapid thermal anneal at 400 °C. The detachment is induced by porous interface (H-platelets) and stress in the layer [4]. The epifree layer was obtained by the formation of a detachable uniform and continuous film from a monocrystalline silicon wafer. The details of the complete process are described in ref. [10]. HIT solar cell structures were fabricated on the 280 μm nanopatterned wafers and 25 μm c-Si wafer with an emitter consisting of a 25 nm a-SiC:H/a-Si:H/(n+) a-Si:H stack deposited by PECVD [4]. To complete the structure, the back stack consisting of a-SiC:H/a-Si:H/(p+)a-Si:H films was deposited by the dissociation of trimethylboron TMB and SiH_4. The active solar cell area of 1 cm^2 was defined by sputtering ITO through a shadow mask followed by an Al grid contact evaporated through a shadow mask. Back contacts were also formed by Al evaporation.

The effect of the nanopatterning on the electronic properties was quantified by means of the effective minority carrier lifetime (τ_{eff}) deduced from the photoconductance measured with a Sinton WCT-120s setup. The effective lifetime reflects the recombination processes in the bulk and at the surfaces and is defined as follows [23]:

$$1/\tau_{eff} = 1/\tau_{bulk} + (S_{Front} + S_{Back})/d \quad (1)$$

where τ_{bulk} is the bulk lifetime, d is the thickness of the substrate, and S_{Front} and S_{Back} are the recombination velocities in the front and the back surfaces, respectively. We used a 280 μm reference wafer to calculate the recombination velocity on a flat surface, assuming that τ_{bulk} is infinite and that the passivation is symmetrical at the front and back surfaces. Then we have calculated the surface recombination velocity for the nanopatterned surfaces for the wet and dry sample as:

$$S_{np} \approx d/\tau_{eff} - S_{flat} \quad (2)$$

where S_{flat} and S_{np} are the recombination velocities for the flat and nanopatterned surfaces, respectively. Due to the limitation of sample size requirement for the photo-conductance technique ($>20\ cm^2$) the surface passivation of ultrathin c-Si layers was characterized by time-resolved microwave conductivity (TRMC) measurements. In TRMC, the sample is excited using a laser pulse ($\lambda = 532$ nm) over an area around 1 mm^2. The pulse creates an excess of minority charge carriers leading to a change of the sample conductivity which temporarily modifies the optical properties of the material in the terahertz spectrum. The relative minority carrier lifetime is related to the transients by the time constant of the exponential decay. In addition, the topography of the nanopatterned wafers was studied by scanning electron microscopy (SEM) and the spectral total reflectance was measured using an integration sphere in the wavelength range from 300 to 1100 nm. The solar cell parameters of the HIT structures were extracted from current–voltage measurements under AM1.5G illumination and external quantum efficiency (EQE) measurements.

3. Experimental results and discussions

Fig. 1 shows an SEM top view of the final patterns on the (1 0 0) FZ c-Si wafers for wet (Fig. 1a) and dry etched (Fig. 1b) samples. TMAH wet chemical etching is based on the different etch rates for the (1 1 1) and (1 0 0) crystallographic planes. This chemical treatment of the (1 0 0) oriented c-Si substrate, protected by the NIL SiO_2 hard mask, produces a periodic array of inverted nanopyramids with the (1 1 1) crystallographic orientation of walls and a base angle of 54.7°. On the other hand, dry plasma etching is independent of the crystal orientation, and as a result, parabolic shapes were obtained on the c-Si surface. The final patterns have a depth of 300 nm and diameters of 300 nm and 500 nm for dry and wet etching, respectively. As a result of the dry etching process, the sidewalls of the

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