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Kerfless layer-transfer of thin epitaxial silicon foils using novel multiple layer porous silicon stacks with near 100% detachment yield and large minority carrier diffusion lengths

Hariharsudan Sivaramakrishnan Radhakrishnan [a,*], Roberto Martini [a,b], Valerie Depauw [a], Kris Van Nieuwenhuysen [a], Twan Bearda [a], Ivan Gordon [a], Jozef Szlufcik [a], Jef Poortmans [a,b,c]

[a] IMEC vzw, Kapeldreef 75, B-3001 Heverlee, Belgium
[b] Department of Electrical Engineering, KU Leuven, Kasteelpark Arenberg 10, B-3001 Heverlee Belgium
[c] Universiteit Hasselt, Campus Diepenbeek, Agoralaan - gebouw D, B-3590 Diepenbeek, Belgium

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ABSTRACT

Two important aspects for the success of the porous silicon-based layer transfer method in producing kerfless thin (<50 μm) silicon foils for future silicon solar modules are addressed in this work: achieving high detachment yield and high minority carrier diffusion lengths. The detachment characteristics of the porous silicon-based lift-off process is studied using finite element modeling as well as experiments. It is shown that for easy detachment and high detachment yield, a low density of thin silicon pillars must be attained in the high porosity detachment layer (HP-DL) after high temperature sintering. This is elegantly achieved by increasing the thickness of the low porosity template layer (LP-TL) which acts as the vacancy supply to increase the post-anneal porosity of the HP-DL. In this way, near 100% detachment yield has been achieved. However, a thicker LP-TL results in a poorer quality epitaxial growth surface. To circumvent this trade-off, novel triple and quadruple layer porous silicon stacks are introduced which decouple the function of the LP-TL that acts as both the template for epitaxy and as the vacancy supply for the HP-DL. In these new stacks, a surface zone of very low void size and density (nearly void-free) is created which allows high quality epitaxy on easily-detachable porous silicon stacks. Minority carrier lifetime measurements on epitaxial foils grown on such a triple layer stack has resulted in an effective lifetime of $\sim$350 μs at the injection level of 10^{15} cm^{-3} which corresponds to a minimum minority carrier diffusion length of $\sim$670 μm ($>$ 16 times the silicon thickness). With such high quality epitaxial foils combined with high detachment yield, very high efficiency solar devices on thin silicon substrates would be a reality in the near future.

1. Introduction

The cost of silicon (which is the sum of useful silicon used in cell processing and the silicon lost in the kerf during wire sawing of silicon ingots into wafers) constituted a significant 32% of the total cost of silicon solar modules in 2014 [1]. Thus, there is a strong motivation to reduce the cost of silicon in silicon solar cells. Kerf-less layer transfer of epitaxial thin (<50 μm) silicon foils ("epifoils") using porous silicon as the detachment layer reduces the amount of silicon used per m^2 and hence potentially the cost of silicon solar modules fabricated in this route. Presently, there is a lot of exciting research on-going both in the production of such thin silicon and their use in fabricating high-efficiency silicon solar cells and modules [2–7].

An example of a processing sequence based on the porous silicon-based layer transfer method is depicted schematically in Fig. 1. Firstly, a stack of porous silicon is electrochemically-etched on the surface of a highly boron-doped wafer in a HF-based electrolyte. The standard porous silicon stack used today is a double layer of 250–300 nm-thick high porosity detachment layer (HP-DL) underneath a 1–2 μm-thick low porosity template layer (LP-TL) [8–10]. After etching, the sample is annealed at a high temperature ($\geq$1100 °C) in hydrogen ambient [4,9,10], which results in the sintering of porous silicon leading to the formation of a detachment plane in the HP-DL and a well-closed LP-TL surface suitable for the following in-situ epitaxial growth of silicon. Note that the detachment layer (DL) and the template layer (TL) have also been called as the separation layer and starting layer, respectively, in literature [8,11]. After epitaxy, the front-side

Abbreviations: BDT, brittle-to-ductile transition; DL, detachment layer; FEM, finite element modeling; HP-DL, high porosity detachment layer; LP-TL, low porosity template layer; TL, template layer

* Corresponding author. Tel.: +32 16 28 1173/32 488 29 28 32.
E-mail address: sivarama@imec.be (H. Sivaramakrishnan Radhakrishnan).

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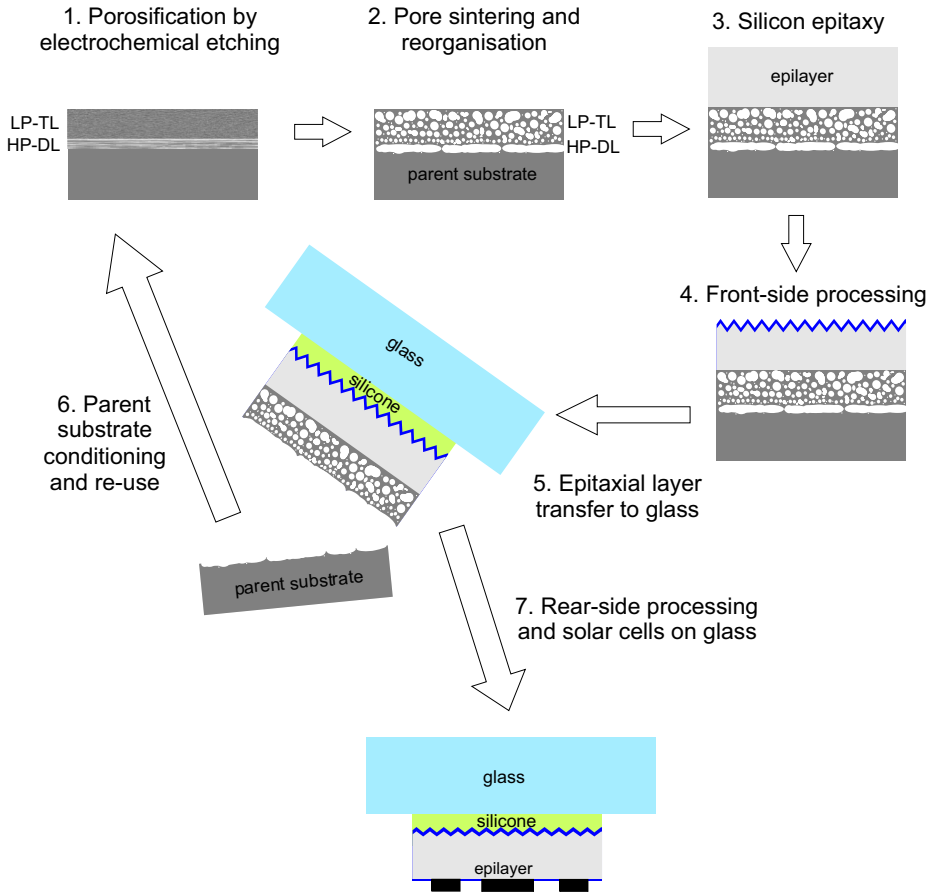

Fig. 1. The process flow for the fabrication of a layer-transferred epitaxial silicon solar device, showing the details of the porous silicon-based layer transfer process. Note the schematics are not drawn to scale. In particular, the epitaxial layer and porous silicon stack have been exaggerated for clarity.

of the epitaxial layer is processed (e.g. texturing, deposition of anti-reflection coating and passivation) while it is attached to the parent silicon substrate. Subsequently, the front side-processed epitaxial film is bonded to glass using silicone as gluing material. A small mechanical force then allows the detachment of the epitaxial layer from the parent substrate at the DL, thus transferring the epitaxial layer (now called an "epifoil") to glass. Alternatively, the epitaxial film may also be detached as a free-standing foil before bonding to glass but, in this case, the handling of the fragile free-standing foil may be problematic. Finally, the rear-side of the epitaxial foil is processed at the module level into a solar device (e.g. emitter patterning, passivation and metallization), and the parent substrate is conditioned for the re-use in the next cycle of layer transfer. In this process sequence, porous silicon is crucial as the enabling technology for the production through layer transfer of very thin epitaxial silicon. Equally as important is its role as a seed layer for the high quality epitaxial growth of silicon.

The world record in efficiency of 20.62% for thin epitaxial solar cells, obtained using thin silicon foils from the porous silicon-based layer transfer approach, has been achieved by Solexel [5], indicating the high potential of this concept. However, there are two critical aspects integral to the success of layer-transferred epitaxial silicon solar cells. Firstly, a yield for the porous silicon-based detachment step of nearly 100% must be attained. Secondly, the porous silicon stack must be optimized to allow high quality epitaxy on its surface. It is shown in this work that there exists a trade-off between these two aspects. This article addresses both challenges and proposes a practical solution to circumvent the apparent trade-off in order to achieve both high quality epitaxial foils and high detachment yield simultaneously.

2. Material and methods

2.1. Finite element modeling of the detachment process

Three-dimensional (3D) finite element modelling (FEM) using COMSOL Multiphysics 4.3a was used to study both the detachment characteristics and the influence of pillar size and pillar density on the detachment yield. The set-up used for simulation is similar to that used in [12] and is shown in Fig. 2 (a) and (b), where the silicon pillars are approximated as cylindrical rods with chamfered edges and the LP-TL is taken to be similar to bulk silicon for simplicity. The pillars are regularly spaced and of uniform size. The corresponding cross-sectional scanning electron microscopy (SEM) image of the porous silicon stack that is modelled is shown in Fig. 2 (c). Where it is not mentioned, a silicon stripe of 1 μm is used in the simulations with a peeling force of 50 nN applied to the edge of the epitaxial film. This corresponds to a small force of 5 mN for a epitaxial film with an edge length of 10 cm. Tetrahedral meshing elements were used and the mesh density was controlled automatically such that a fine mesh is achieved in the narrow regions around the silicon pillars for greater accuracy in the calculations.

2.2. Experimental methods

Samples for both detachment studies and minority carrier lifetime measurements are prepared in a similar manner to the sequence shown in Fig. 1 and explained in Section 1. The methodology for the preparation of samples for lifetime measurement has already been detailed in [10,13]. Here, a recapitulation with additional details is provided.