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Novel texturing process for diamond-wire-sawn single-crystalline silicon solar cell

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ABSTRACT

An urgent challenge to popularize diamond-wire-sawn single-crystalline silicon (DWS *sc*-Si) wafers to PV industry is to develop a proper texture process, specially eliminating its severe saw marks and forming uniform pyramid texture. Using a simple pre-polishing step with TMAH plus routine texture process, the saw marks as well as amorphous silicon layer are removed effectively, thus benefiting the formation of a random pyramid structure on DWS *sc*-Si wafers, and the texturing mechanism beyond was discussed. With new texture surface, DWS *sc*-Si cells demonstrated similar reflection ~5% and same efficiency level ~19.15% to the traditional multi-wire-slurry-sawn solar cells. The techniques present in this article can be easily scaled up in PV industry.

1. Introduction

In last decades, the multi-wire-slurry-sawing (MWSS) is a mainstream technique to slice large ingots of single/multi-crystalline silicon into thin wafers in PV industry [1,2]. However, some shortages of MWSS emerge seriously: environment contamination, low productivity, high breakage of steel-wire and material consumption [3,4]. To solve those problems, a new silicon wafer cutting method called diamond-wire sawing (DWS) was raised to replace MWSS by many relevant research groups [5,6]. DWS technology, featured as the higher productivity, lower wear of the wire, and easier recycling of the cooling liquid [7], is expected to become the mainstream technique for cutting the silicon ingots.

However, DWS is not adopted extensively by PV industry because that the normal texture process for MWSS *sc*-Si wafers based on isotropic alkaline etching isn't fully competent for DWS ones [8–10]. The surface differences between MWSS and DWS *sc*-Si wafers is obvious: the former features a thicker damaged layer (~10 μm) with random distribution of broken crystals, which are uniform to the etching solutions; the latter has a damaged layer (~5 μm) covered by ~10–20 nm amorphous silicon induced by high-speed cutting of the diamond particles adhered in the wire, and there are a lot of parallel saw marks and hard damaged pits remained on the wafer surface, which are certainly nonuniform to the texturing solutions. Under normal texture process, it was reported that the amorphous silicon layer, confirmed by Raman spectroscopy, will hinder further etching process [11], meanwhile those areas covered by random distributed pits will be etched easily. Consequently, the high reflectivity and serious saw marks will decrease cell's efficiency (η).

It is urgently challenge to solve the texturing problems in aim to popularize DWS sc-Si wafers in PV industry. Usually, only a simply pre-treatment with SC-2 ($HCl+H_2O_2+H_2O$) clean process was applied for the commercial Si wafers. After that, photovoltaic production widely uses potassium hydroxide (KOH) or sodium hydroxide (NaOH) as aqueous texturing solutions to remove saw damage layer before etching the silicon surface anisotropically into small pyramids; Besides, acidic-based solution such as $HF:HNO_3$ can also remove the saw damage surface [12,13]. However, we found that they are incapable to erase saw marks on the surface of DWS *sc*-Si wafer. As a clean room compatible, nontoxic and easy to handle solution, tetramethylammonium hydroxide ($(CH_3)_4NOH$, TMAH) with low concentration less than 15 wt.% is extensively reported and used as the texture solution for the formation of pyramids on silicon wafer [14,15]. More interesting for us, a 25 wt.% TMAH can drastically reduce the surface roughness of silicon wafer [16], and is quite promising to remove the saw marks on the surface of DWS *sc*-Si wafer.

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In this study, we report that both the saw marks and amorphous layer on the surface wafer can be erased largely through a TMAH pre-polishing, thus benefiting the formation of uniform pyramidal structure under a routine texture process, and the DWS *sc*-Si cells can realize the same reflection and efficiency to MWSS ones in the same production line.

2. Experiments

In this article, (1 0 0) *sc*-Si wafers ($15.6 \times 15.6 \times 0.018\ cm^3$) were cut by DWS and MWSS from same *sc*-Si ingot made through Czochralski method. First, both DWS and MWSS *sc*-Si wafers were applied a routine texture process of production line in a solution consisting of 2% NaOH, commercial additives and H_2O to observe the microstructure development during the etching process. However, such routine etching process is incapable to form efficient texture for DWS *sc*-Si wafer, as will be presented in next section. Second, a novel texture process was developed to texture DWS *sc*-Si wafer by adding a TMAH polishing step prior to the routine etching process. Third, above wafers were assembled into solar cells in a pilot line at Canadian Solar Inc. (CSI) @ Suzhou by using a standard process including the phosphorus oxychloride diffusion in tube furnace at a peak temperature of 870 °C, the removal of edge and back *pn* junctions with Inoxide RENA, the antireflection coating of silicon nitride (SiN_x) through plasma-enhanced-chemical-vapor-deposition (PECVD) with Roth&Rau, and the screen printing/co-firing of both rear contact of aluminum layer and the front finger and busbar of silver by using a pattern of 91 grid lines, and the PV17F Ag paste bought from DuPont Co.. Both flow charts for wafer's texture and cell's fabrication are shown in Fig. 1.

The reflection was measured with standard diffusion 8° integration sphere spectroscopic-reflectometer (D8) between 350–1050 nm. The reaction evolution of DWS wafers was investigated by Hitachi S-4800 FEG SEM to record the variations of surface structure after employing different etching durations from 100 s to 900 s. The μ-PCD function of Semilab WT-2000PV was used to measure the effective lifetime after texturing. The phosphorus dopant profiles, external/internal quantum efficiency (EQE/IQE), and surface sheet resistance were measured by secondary ion mass spectroscopy (SIMS), PV Measurements (QEX7, USA), and 4 Probe sheet resistance tester (Napson RT-70V, Japan), respectively. The efficiencies of cells were measured under AM 1.5G illumination through IV measurement system (Berger PSL-SCD, Germany), and calibrated with the standard cells of Fraunhofer Institute for Solar Energy Systems, Germany.

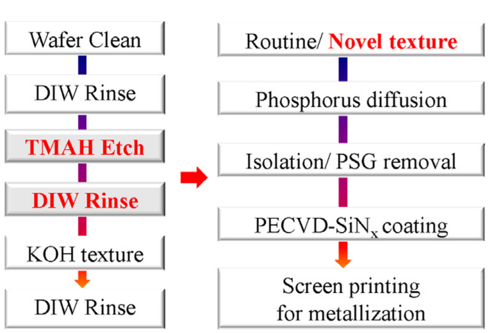

Fig. 1. Flow charts of routine/novel wafer texture process (left) and cell fabrication process (right). For novel texture process, a TMAH pre-polishing step was added into routine one. The fabrication process for MWSS and DWS cell is same.

3. Results and discussions

3.1. Surface characterization of as-cut DWS sc-Si wafer

Initial surface microstructure of DWS *sc*-Si wafers is critical important for forming proper surface texture under etching solution. Fig. 2 compares the SEM images of as-cut MWSS and DWS *sc*-Si wafers. MWSS wafer surface has randomly distributed microcracks and fractures due to a rolling-indenting model [2]. In contrast, the surface morphology of DWS *sc*-Si features as the parallel saw marks/grooves, the disperse pits, and the amorphous layer (~20 nm) due to ductile cutting model [17,18], and its typical microstructures are highlighted in the Fig. 2a) and b). Interesting, there are two types of grooves that are evident on the surface. The shallow grooves (~1 μm in depth) are formed with a layer of amorphous silicon (and sometimes also metastable phases) when the silicon ingot was scratched by diamond grits with a normal motion at a low load [9]. The deep grooves (> 3 μm in depth) occur when the diamond wire stops and reverses direction [19], at the moment the diamond grits will place an extra force to the silicon surface, thus introduce a lot of defects in there. Particularly, we propose that the saw marks are the visual contrast effect among deep and shallow grooves. As a result, DWS *sc*-Si wafer has much higher initial reflection to the MWSS one (36% vs. 28%).

3.2. Etching DWS sc-Si wafer with a routine texture process

A routine texture process of *sc*-Si wafer has two main purposes, that is, removing the damaged surface layer, and further forming pyramid texture on the surface and the chemical reaction between silicon and NaOH is,

$$Si + 2NaOH + H_2O = Na_2SiO_3 + 2H_2\uparrow$$

The alkaline etching process leads to the anisotropic formation of {1 1 1} pyramidal structures, which can be explained by back-bond breaking theory [20,21], and its geometries allow light to be more easily coupled into the silicon solar cell. In fact, the etching kinetics is much complicated due to several facts, that is, surface conditions, temperature, H_2 adhere to the surface. In order to control the size and density of the resulting pyramids, a lot of additives have been developed in the past decades with functions to remove H_2 bubbles adhere to the surface, to enhance the pyramid nucleation by improving the wettability of the wafer surface, and to tune reaction speed [22,23].

In this work, a texturing solution containing 1% NaOH and 0.3% commercial additive was first used for etching both DWS and MWSS *sc*-Si wafers. The additive (TS41, Changzhou Shichuang Energy Technology Co. Ltd., China) containing several solvents, such as sodium hydroxide, ascorbic acid, sodium benzoate, high-efficient defoaming agent and surface cleaning agent, has been verified suitable for texturing MWSS *sc*-Si wafer to achieve an efficiency ~19%. After 900 s etching, uniform pyramids of a peak size distribution at 3–5 μm are obtained in MWSS *sc*-Si wafer, whereas the saw marks are still visible for DWS *sc*-Si wafer. The etch thickness of wafer can be calculated by measuring its mass loss during texturing process. For instance, the MWSS *sc*-Si wafer is etched 5μm each side (~0.55 g mass loss), while 2.7 μm each side for DWS *sc*-Si wafers (~0.31 g mass loss). The results confirm that the dissolution speed of silicon of DWS wafer is much slower than that of MWSS one under same etching solution.

To clarify the etching behaviors of DWS wafer, the surface and cross-section SEM images of DWS wafer after 500 s and 900 s routine texture process are presented in Fig. 3. After a short etching time of 500 s, some of pyramids appeared in the deep