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Cadmium sulfide nanowire arrays for window layer applications in solar cells

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ABSTRACT

Arrays of 100 nm long n-cadmium sulfide (CdS) nanowires were investigated as replacement for the planar n-CdS film, which is presently used as a window layer in many solar cell devices. These arrays exhibited substantial transmission at wavelengths below 512 nm. Theoretical calculation involving the number of extra photons transmitted through the CdS nanowire window layer indicated a potential enhancement in photocurrent by 20.6% and in open circuit voltage by 10.2% over the device using planar CdS film as the window layer. Next, Au/CdS Schottky diodes were formed. Analysis of the current–voltage characteristics of these Schottky diodes showed smaller diode ideality factors and higher current density in devices with CdS nanowires than in devices with planar CdS film. Capacitance–voltage measurements yielded values of effective carrier concentration ($N(x)$) in the CdS nanowire. $N(x)$ varied along the length of nanowire; it was higher near the top surface and lower, near the S_nO_2 base. In initial experiments, p-CdTe layer was deposited on top and a nanowire-CdS/CdTe photovoltaic device of 0.04 cm^2 area exhibited short current density (J_{sc}) of 25.8 mA/cm^2, open circuit voltage (V_{oc}) of 722 mV and fill factor of 52.8%, resulting in an a power conversion efficiency value of 9.8%.

1. Introduction

Cost-effective photovoltaic (PV) technologies are the key for large-scale deployment of solar cells. Devices based on thin film semiconductor materials like cadmium sulfide (CdS), cadmium telluride (CdTe), and copper–indium–gallium–diselenide (CIGS)) are promising because of their significantly lower manufacturing costs and high power conversion efficiencies. However, when trying to maximize device performance, improvements have been hindered by the loss of photocurrent caused by light absorption in the n-type cadmium sulfide (CdS) window layer. Due to a high density of recombination sites in CdS films, a significant amount of radiation in the solar spectrum, with wavelength less than 512 nm, gets absorbed in CdS but does not contribute to the collected photocurrent. The resulting loss in photocurrent is estimated to be 7 mA/cm^2 [1]. Also, forming a thinner layer of CdS, less than 100 nm thick, to reduce its absorption presents significant challenges of its own, because it tends to result in the formation of pinholes in CdS. These pinholes can cause the p-type semiconductor (CdTe or CIGS) to come in direct contact with the transparent electrode (ITO, for example), thus forming micro-junctions and micro-shunts and degrading cell performance.

CdS and CdTe nanowire arrays with radial or axial p–n junctions are being explored as an alternative to CdS and CdTe thin films for photovoltaic applications. The wire arrays can, in principle, provide more effective photon absorption in the absorber semiconductor and also more efficient carrier collection [2–14].

Earlier, Guduru et al. reported on Schottky diodes on CdS nanowires [15]; however the length of CdS nanowires in their work was much higher than 100 nm and therefore not suitable for window layer applications in solar cells like CdS/CdTe and CdS/CIGS.

Fan et al. [4,8] developed three dimensional, single crystalline n-CdS nanopillars, embedded in polycrystalline thin films of p-CdTe to enable efficient collection of carriers. These radial p–n junction cell geometries grown by the VLS method exhibited power conversion efficiency values of up to 6%. However, Au catalyst atoms used in the VLS method can diffuse into the p-type absorber. Gold atoms form deep level trap states in the p-type absorber which act as efficient SRH recombination centers, reducing minority carrier lifetime and degrading device performance [8]. Also, the length of n-CdS nanopillars was rather large,

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about 1 μm; this would lead to substantial loss in photocurrent due to absorption of light in the CdS pillars.

To achieve higher power conversion efficiency values, the CdS nanowire arrays must transmit a large number of sunlight photons that can reach the absorber semiconductor layer and be converted into electrons and holes there. Device configuration presented in this paper achieves that goal. Also, the fabrication process does not involve a metal catalyst and the problems associated with the metal diffusion are circumvented. Furthermore, our device configuration employs a transparent, conductive substrate, which makes it easy to illuminate the p–n junction and Schottky diode devices through the substrate. Fabrication and electro-optical characterization of these device configurations are described in the following sections.

2. Experimental procedures

Nanowire arrays were fabricated by the electrodeposition of CdS into nanoporous membranes of anodized aluminum oxide (AAO). The procedure for preparing the AAO membranes [13] involved sputtering on top of the commercially purchased ITO–glass substrate, a 100 nm thick SnO_2 and a 5 nm thick titanium layer and then depositing a 100 nm (or 200 nm) thick aluminum film by electron beam evaporation. The anodization of thin (100 nm or 200 nm thick) aluminum films was conducted in 0.3 M oxalic acid under constant voltage of 50 V and a current of 0.1 A where temperature of electrolyte was 5 °C. Then, these samples were etched in 5% phosphoric acid for 30 min at room temperature, followed by a reactive ion etch (RIE) process for 2 min to completely remove the aluminum oxide barrier layer at the base; during RIE, RF and ICP power were set at 90 W and 250 W respectively. From scanning electron microscopy (SEM) analysis, the area density of pores was found to be 1.14×10^{10} cm^{-2}; average pore diameter was 60 nm; average distance between the centers of neighboring pores was 106 nm and the fraction of total surface area covered by the pores was 0.32.

For the CdS nanowires deposition, the electrolyte was a mixture of 0.055 M cadmium chloride ($CdCl_2$) solution and 0.19 M elemental sulfur in 50 mL dimethyl-sulfoxide (DMSO) solution. Nominal current density over the sample area during electrodeposition was set at7 mA/cm^2, and the deposition temperature was maintained at 140 °C. Nominal current density calculation was based on the total surface area of the AAO membrane, which included the pores as well as the embedding aluminum oxide matrix. If only the pore areas were to be considered because the CdS electrodeposition actually occurs only in the pores, then the "actual" plating current density inside the pores would be $7.0/0.32=21.9$ mA/cm^2. Following growth, the CdS nanowires were treated with 75%-saturated $CdCl_2$ (methanol solution) for 15 min and annealed at 400 °C for 30 min with 100-sccm Argon purge.

In preparation for Schottky diode fabrication, the annealed samples were etched with 1 N NaOH solution for 2–3 min. The NaOH solution does not react with CdS nanowires and is highly selective to remove AAO template. The duration of 2–3 min NaOH etching resulted in the top 20–30 nm portion of the CdS nanowires getting exposed while the rest of CdS nanowire length remained embedded in the AAO matrix. This step was needed because, to make robust Schottky diode contact (gold) to the embedded CdS nanowires, it is essential that all nanowires be flush with or slightly protruding above the plane of the embedding AAO matrix. In other words, CdS nanowires were exposed so they would, later, make a clean contact with the vacuum evaporated gold layer.

For comparative evaluation, planar CdS films were fabricated on top of 100 nm SnO_2/ ITO/glass substrates by the traditional chemical bath deposition method [16]. Following same heat treatment procedure as for the Nanowire-CdS film, planar CdS was treated with 75%-saturated $CdCl_2$ and then annealed at 400 °C for 30 min with 100-sccm Argon purge.

After $CdCl_2$ treatment and annealing, Schottky diodes were made by depositing Au contacts by thermal evaporation on top of the nanowire-CdS films as well as the planar CdS films. These contacts were circular dots of diameter, 1/8 in. and area, 0.07 cm^2.

In preliminary experiments on solar cell fabrication, bulk p-type CdTe layers were deposited on top of the embedded CdS nanowires. This was done in a closed-space sublimation system, where source and substrate were ramped together to 550 °C. Then source temperature was increased to 625 °C and held there for 2 min at 15 Torr pressure of He (with 5% O_2, as background gas) pressure. After CdTe deposition, the cells were treated with 75% $CdCl_2$ methanol solution for 15 min and were annealed at 400 °C for 30 min in 100-sccm Argon. This annealing of CdTe in the presence of cadmium chloride was essential for achieving good performance in terms of open circuit voltage and fill factor of the photovoltaic device. Next, cells were etched in a mixture solution of nitric acid and phosphoric acid (1% HNO_3, 88% H_3PO_4, 35% DI-water) for 35 s to form a thin tellurium rich (Te+) layer [16]. Then, a thin layer of copper, 5 nm in thickness, was sputtered on the surface of CdTe at the back contact area sites. This was followed by the application of graphite paste–silver paste electrodes.

Material and optical–electrical characterizations were performed on the samples of CdS nanowires and planar CdS films, which had been subjected to $CdCl_2$ treatment and annealing. Material characterization was conducted with the techniques of X-Ray diffraction (Bruker-AXS D8 DISCOVER Diffractometer), and scanning electron microscopy (Hitachi S-900 field emission SEM). Optical transmittance spectra were measured with a Cary, Model 50 Probe UV–Visible Spectrophotometer over a wavelength range of 300–800 nm.

Electrical properties of the Au/CdS nanowire Schottky diodes and nanowire CdS–CdTe solar cells were characterized by current–voltage (*I–V*) and capacitance–voltage (*C–V*) measurements. *I–V* characteristics were measured using a solar simulator in the dark and under illumination intensity of 100 mW cm^{-2}; solar simulator was calibrated with a standard light meter and with a standard crystalline silicon solar cell. *C–V* characteristics were measured with an Agilent 4284A capacitance meter (Agilent Technologies; 20 Hz to 1 MHz) at a frequency of 1 MHz; during capacitance measurement, the Au contact on CdS nanowires was biased positive relative to ITO; d.c. bias voltage ranged from −1.0 V to 1.0 V.

3. Results and discussion

3.1. SEM and XRD characterization

Fig. 1(Left) and Fig. 1(Right) show the top view and cross sectional view, respectively of scanning electron microscope (SEM) images of CdS nanowires. Pores are completely filled with CdS and nanowire arrays are uniform and dense; length of nanowires is 100 nm; average diameter is 60 nm and the average distance between the centers of neighboring nanowires is 106 nm. Porosity and area density of CdS nanowires were calculated as 32% and 1.14×10^{10} nanowires/cm^2 respectively. These high density CdS nanowire arrays are seen to be growing perpendicular to the conductive TCO/glass substrate and are well aligned. It should be noted that such well-aligned rows and columns of nanowire arrays produced from the periodic arrangement of AAO membranes are