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Impact of metal-organic vapor phase epitaxy environment on silicon bulk lifetime for III–V-on-Si multijunction solar cells

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ABSTRACT

With the final goal of integrating III–V materials on silicon substrates for tandem solar cells, the influence of the metal-organic vapor phase epitaxy (MOVPE) environment on the minority carrier properties of silicon wafers has been evaluated. These properties will essentially determine the photovoltaic performance of the bottom cell in a III–V-on-Si tandem solar cell. A comparison of the base minority carrier lifetimes obtained for different thermal processes carried out in a MOVPE reactor on Czochralski silicon wafers has been carried out. An important degradation of minority carrier lifetime during the surface preparation (i.e. H_2 anneal) has been observed. Three different mechanisms have been proposed for explaining this behavior: (1) the introduction of extrinsic impurities coming from the reactor; (2) the activation of intrinsic lifetime killing impurities coming from the wafer itself; and finally, (3) the formation of crystal defects, which eventually become recombination centers. The effect of the emitter formation by phosphorus diffusion has also been evaluated. In this sense, it has been reported that lifetime can be recovered during the emitter formation either by the effect of the P on extracting impurities, or by the role of the atomic hydrogen on passivating the defects.

1. Introduction

Multijunction solar cells (MJSCs) are one of the most successful device architectures to implement ultra high efficiency photovoltaic devices. More specifically, the combination of III–V compounds and silicon (Si) in hybrid MJSCs represents a long sought for device that would link the already demonstrated efficiency potential of III–V semiconductor MJSCs with the low cost and unconstrained availability of silicon substrates. The ultimate goal is to produce high-efficiency photovoltaic devices, while reducing the cost of solar electricity down to levels competitive with conventional sources.

Among the many alternatives followed for III–V on silicon integration [1], one of the most successful approaches so far investigated consists on the metamorphic integration of III–V semiconductors (GaAsP or GaInP) on a Si bottom cell, through the use of a GaP nucleation layer. This layer acts as a defect-free III–V template on Si [2–6], onto which a GaAsP graded buffer, which aims to confine the propagation of structural defects (i.e. threading dislocations), can be integrated. In this virtual substrate, GaAsP or GaInP top cells can be eventually integrated, thus forming a GaAsP/Si [7–11] or a GaInP/Si [12] MJSC. The vast majority of the efforts of the different groups trying to materialize this strategy have been directed towards the optimization of key steps in the epitaxial growth of III–V compounds on Si, such as the nucleation layer (GaP), the graded buffer (GaAsP) and the top subcell (GaAsP/GaInP) [6,9,11]. The main target has been the minimization and confinement of crystal defects in the structure. In this sense, high structural-quality graded buffers have been reported, achieving promising results in the reduction of the dislocation density and in the annihilation of antiphase domains [7,9]. However, no work has been done aimed to understand the consequences of such processes on the photovoltaic performance (i.e. minority carrier lifetime) of the Si substrate, which eventually will act as the bottom subcell of the MJSC. Needless to say, the formation of a high quality bottom cell will be crucial for obtaining a highly efficient multijunction solar cell structure. This optimization requires several items, such as: (a) the preparation of the substrate for subsequent III–V growth, (b) the formation of an emitter with an adequate depth and doping concentration in the silicon bottom subcell, and (c) the attainment of a sufficiently high minority carrier lifetime in the base of the silicon bottom subcell. The latter is a key feature since the bottom cell base minority carrier parameters will determine the PV performance of the bottom subcell in the tandem stack [13]. It is well established that the minority carrier lifetime in conventional PV silicon processing is not a constant material property but depends strongly on the thermal history and the environment where the sample was

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processed [14]. Analogously, a strong influence of the metal-organic vapor phase epitaxy (MOVPE) environment on this parameter has been reported by us elsewhere [15].

In this paper we will present results about minority carrier lifetime evolution in the MOVPE processing of silicon substrates for III/V-on-Si photovoltaics. Essentially two alternatives have been proposed in the literature for this processing or, more in particular, for the formation of the silicon subcell emitter. The first one is based on the homoepitaxial growth of silicon on the Si substrate [3,6]. This implies either the need for a special MOVPE reactor able to grow both group IV and III–V compounds (i.e. specially designed to minimize cross-contamination and carry over effects), or to grow the structure in a two-step process (i.e. taking the samples out of the reactor after Si growth, cleaning the reactor, and loading again for III–V growth). The use of homoepitaxial growth of Si has demonstrated to be a beneficial factor in the production of high quality GaP-on-Si layers [3,6], though, as discussed, introduces an additional degree of complexity in the epitaxial process. A simpler alternative would be to mimic what is done in conventional MJSC technology on germanium substrates, where the bottom subcell emitter is formed by diffusion of phosphorous (P), resulting from the pyrolysis of phosphine (PH_3). In this respect, it should be noted that several groups have also reported high quality GaP layers without homoepitaxial silicon buffers [2,9]. Accordingly, in this work we will focus on this strategy and consider the formation of the emitter from diffusion as is the case in conventional III–V triple-junction solar cells based on germanium.

In summary, in this paper we will study the evolution of the minority carrier lifetime in the silicon substrate during the formation of the bottom subcell of a III–V/Si MJSC. In particular, in the diffused emitter approach, this process consists of three steps: (1) In the initial stage of the MOVPE process, wafers are typically subjected to a high-temperature annealing under hydrogen (H_2) atmosphere to prepare the surface for a high-quality III–V semiconductor epitaxy (oxide pyrolysis, double-step formation, …) [16,17]; (2) in order to form the emitter, wafers are exposed to high-temperature bakes under phosphine (PH_3) to enable the diffusion of phosphorus (P) into the silicon substrate [18]; and (3) finally, as a result of the surface degradation caused by the PH_3 exposure during the formation of the emitter, substrates need to be submitted to an additional treatment, aimed to recover the surface morphology for subsequent epitaxial growth [19]. In this sense, the formation of the emitter by exposing wafers to a high PH_3 concentration is followed by a H_2 annealing intended to recover the damaged surface morphology. Therefore, the impact on the base minority carrier lifetime of these three processes and environments will be assessed in this paper.

2. Experimental

The substrates used for this work were p-type boron-doped Czochralski (Cz) Si wafers oriented (100) with a miscut of 2° and 6° towards the nearest (110) plane (both misorientations were investigated). Unless otherwise is specified, the resistivity of the wafers is 5–10 Ω cm. This kind of wafer is the mainstream product for microelectronic and single-crystal PV industries and thus offers the maximum potential for implementing low-cost III–V-on-Si technology. Before loading wafers into the reactor, they were chemically etched, as detailed in Section 3.1, for removing the native silicon oxide and possible external contaminants. The experiments were carried out in a horizontal, research-scale MOVPE reactor, equipped with an IR-lamp heater. All the quartz and graphite components in the reactor chamber were installed clean and heated at 850 °C before the experiments. The carrier gas was Pd-purified H_2, and the P precursor used was high purity PH_3. During the experiments, the phosphine partial pressure was varied from 0 to 32 mbar and the temperature range explored was from 800 °C to 830 °C. In order to crosscheck the results, some experiments were repeated in a different reactor: a close coupled showerhead (CCS) MOVPE reactor, located at the Ohio State University (OSU). Before performing minority carrier lifetime measurements, wafer surfaces were passivated in order to reduce the surface recombination and enable an accurate bulk material minority carrier lifetime measurement. For wafers processed only under H_2 (no P diffusion and thus, no emitter), samples were dipped in HF and then passivated using a 0.05 M quinhydrone-methanol solution as the passivating agent [20]. For samples treated under phosphine, surface layers were removed with an acidic etch consisting in a HNO_3:H_2O:HF solution (to eliminate the P-diffused layer) and then were passivated using the above mentioned wet method. Minority carrier lifetime was measured on the wafers using the well-known Photoconductance Decay (PCD) technique.

3. Results

3.1. Impact of surface preparation

The effect of the surface preparation (i.e. high temperature annealing under H_2) on the minority carrier lifetime was studied elsewhere [15]. Results are summarized in Fig. 1.

As shown in Fig. 1, an important degradation of this parameter was observed after exposing wafers to a high temperature H_2 annealing. However, the origin of this degradation has not been fully understood. Several possibilities were considered initially for explaining this behavior: (a) light induced degradation as a result of the activation of B–O pairs; (b) external contamination present at the wafer surface, which diffuses into the bulk at high temperatures (either present in the *as-received* wafer and not removed in the cleaning or introduced by the MOVPE environment); (c) the activation (i.e. unpassivation) of lifetime killing centers in the Si bulk (initially non-active in the bulk); and finally (d) the formation of crystal defects which eventually become recombination centers. The light induced degradation, enhanced by the activation of B–O pairs, was eventually discarded, since the same results were observed when working with gallium-doped

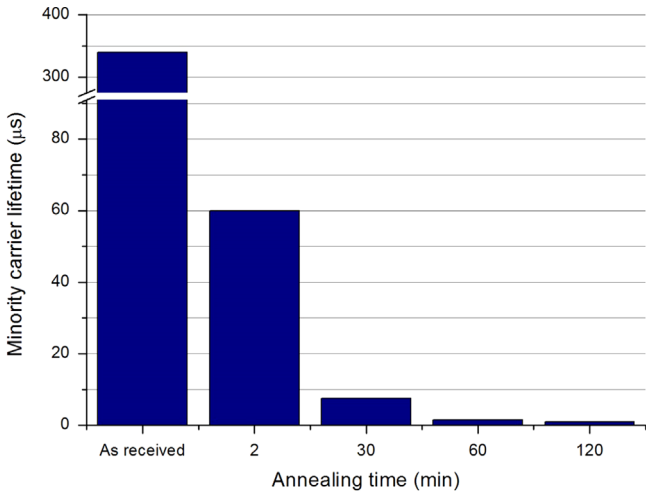

Fig. 1. Minority carrier lifetime for wafers annealed at 830 °C and 900 mbar of H_2 for different times. An *as-received* wafer was included for comparison. Lifetime values were calculated for an injection level of 10^{14} cm^{-3} (except for the *as received* wafer, which was measured for 10^{15} cm^{-3}).