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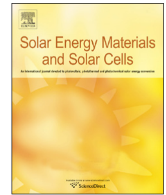

Plasma–silicone interaction during a-Si:H deposition on solar cell wafers bonded to glass

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ABSTRACT

A scenario for future silicon photovoltaics is to use wafer-based solar cells with a thickness below 100 μm. A way to realize this scenario is the merging of cell and module processing, with thin wafers processed while attached to the superstrate glass. One of the challenges for this type of processing is the achievement of high performing surface passivation, i.e., with surface recombination velocities below 10 cm/s. In this paper, a detailed explanation for lifetime degradation on wafers bonded to glass by means of silicone is proposed. The degradation is due to cyclic silicone molecules outgassing during a-Si:H deposition from the adhesive used to bond the wafers. The cyclic molecules are incorporated in the a-Si:H layer and modify the amorphous silicon network. By the application of specific outgassing conditions before a-Si:H deposition, a significant amount of cyclic molecules is removed from the adhesive. Non-degraded a-Si:H layers and surface passivation comparable to standalone wafers are obtained, as shown with measures of lifetime and solar cell open circuit voltage.

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1. Introduction

The use of thin wafers in silicon wafer-based photovoltaics is one of the approaches to reduce the material-per-device consumption of solar modules [1]. Silicon wafers below 100 μm can be directly produced from ingot by different methods [2–4] and high efficiencies have been confirmed on such substrates. State-of-the-art thin wafer-based solar cells have reached values of 19.1% for 43 μm-thick solar cells [5] and 14.9% for 25 μm-thick solar cells [6]. However, thin substrates cannot be processed in standard production lines because of increased wafer breakage that leads to poor production yields.

A method to overcome the issue of wafer breakage is to mechanically support the thin wafer during processing, for example with a wafer carrier. As such, the risk of wafer breakage is limited, but the solar cell process flow must be adapted to the wafer/carrier stack. Literature reveals examples where the final module glass is chosen as a wafer carrier and part of the solar cell processing is performed directly at module level. This is the case for module-level metallization and interconnection [7] in the XIS concept proposed by ECN [8], in the i^2-module concept proposed by IMEC [9] and the 4S concept proposed by ISFH [10]. ISFH also suggests simple module-level screen printed interconnections [11]. Literature also reports examples of solar devices fabricated on thin wafers while they are bonded to different carriers throughout the entire solar cell processing [12–16].

In the proposed IMEC i^2-module approach [17], the starting point is a thick silicon wafer or ingot, the so-called "parent substrate". A few microns at the top of the parent substrate are porosified by means of electrochemical etching. This porous silicon layer is used as a seed for the epitaxial growth of a thin foil that will be processed into a solar cell, and allows the lift-off of this foil from the parent substrate. The front side processing of the solar cell is done while the foil is still attached to the parent substrate [18], whereas the backside processing of the solar cell is done while the foil is bonded to a glass superstrate with a silicone adhesive (Fig. 1). In this way, partial module-level processing is achieved.

In the i^2-module concept, the backside processing is limited to low temperatures because of the presence of an adhesive in the structure. The maximum allowed temperature depends on the

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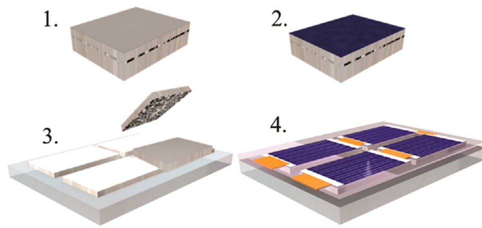

Fig. 1. i^2-Module processing. (1) Thin wafer attached to the parent substrate by means of a porous layer. (2) Frontside processed thin wafer still attached to the parent substrate. (3) Thin wafer(s) flipped and attached to glass by means of silicone. The detached parent substrate is also represented. (4) Backside processed module.

type of adhesive used. Silicone adhesives are used in this work because they can withstand higher temperatures and are more reliable than commonly-used PV encapsulants [19]. However, even for silicones the maximum process temperature is to be kept below 300 °C.

Among the critical process steps of the i^2-module concept, the passivation of the backside of the wafer is fundamental to achieve state-of-the-art efficiency. Literature has reported degradation of passivation if no special care is taken [20]. Some reports also shows high quality passivation of a-Si:H on bonded wafers, with surface recombination velocities below 10 cm/s and comparable to standalone wafers. These results are obtained by tuning the passivation process: either by shielding the silicone [20], or through additional outgassing prior to deposition [21]. However, the phenomena leading to the decay of passivation has not yet been identified.

In this paper, the influence of the outgassing steps on the a-Si:H deposition of bonded wafer is investigated in detail. First the deposited a-Si:H is analyzed in terms of effective minority carrier lifetime uniformity and network structure. Second, the changes in the silicone structure due to the outgassing steps are documented. These analyses are then correlated and the reason for the outgassing step prior to a-Si:H deposition is explained.

2. Methods

The crystalline silicon wafers used in the study are 5×5 cm^2 n-type $< 100 >$ acid-polished FZ silicon wafers with a thickness of 200 μm and a resistivity of 2 Ωcm. The glass substrates are commercially available 700 μm-thick borosilicate glass of an area of 12.5×12.5 cm^2. The silicone adhesive used to bond the wafer to glass is the Dow Corning PV-6100 Cell Encapsulant [22]. This 2-part silicone material is intended for use as a front encapsulant for crystalline Si wafer based PV modules and exhibits suitable optical and physical properties [23]. Three kinds of samples are prepared in this study and are described as follows.

The first type (type I) of samples comprises of bonded wafers for lifetime analysis and are fabricated following the process detailed in Fig. 2. The standalone wafers followed a similar process, except for the steps of silicone application and bonding.

Clean n.1 consists of a 2-step process employing H_2SO_4:H_2O_2 4:1 and HF:H_2O 1:20 and is applied on glasses and wafers separately. After cleaning, the wafers are loaded into a Plasma Enhanced Chemical Vapor Deposition reactor (PECVD) for a-Si:H deposition. The passivation layers consist of 7 ± 1 nm-thick a-Si:H (i) and 18 ± 1 nm-thick a-Si:H(n^+). The a-Si:H(i) layer is deposited at a temperature of 200 °C, a pressure of 1.7 Torr, a power of 50 mW/cm^2 and a silane/hydrogen ratio SiH_4:H_2 of 1:3, while the a-Si:H(n^+) is deposited at a temperature of 170 °C, a pressure of 0.7 Torr, a power of 60 mW/cm^2 and a silane/phosphine ratio SiH_4:PH_3 of 1:1. A H_2 plasma is performed in between the a-Si:H(i) and

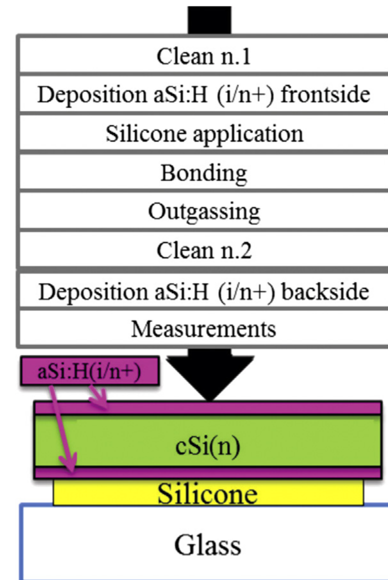

Fig. 2. Process flow (top) and test bonded structures (bottom) used in this study. Standalone wafers and glass/silicone stack without wafer (not shown) are also used.

the a-Si:H(n^+) layer to improve the passivation of the intrinsic layer [24]. The total processing time of the a-Si:H(i/n$^+$) deposition is approximately 15 min, including the steps of loading, temperature stabilization and unloading.

After a-Si:H deposition, approximately 30 μm of silicone are screen-printed on an area of 3.2×4.2 cm^2, both on the wafer and the glass. The thickness of the silicone is determined by a wet film thickness gauge and confirmed by comparing the sample weight before and after screen- printing. The screen-printed area is chosen smaller than the sample area to avoid any passivation degradation due to direct exposure of silicone to the plasma [20,25]. In this way, i.e. shielding the silicone, it is possible to exclusively investigate the effect of the outgassing on the quality of the passivation.

After screen-printing, the samples undergo a curing step of 100 °C for 5 min under vacuum for crosslinking. Compared to the standard curing condition [22], the time is increased from 1 to 5 min. This increase is related to the necessary temperature stabilization time of the vacuum oven used. After curing, the samples are manually bonded and undergo an outgassing step in the same vacuum oven used for silicone curing. The conditions chosen for the outgassing are (A) 15 min, 100°C; (B) 60 min, 100 °C; (C) 15 min, 200 °C; and (D) 60 min, 200 °C. Three samples for each condition are prepared. The outgassing conditions are chosen in order to expose the sample to conditions similar to the ones used during a-Si:H(i/n$^+$) deposition (i.e. approximately 200 °C for 15 min). Temperatures higher than 200 °C are not considered since the sample is not to be exposed to temperatures beyond 200 °C during subsequent processing. However, the study of silicone properties after thermal treatment at temperatures up to 300 °C can be found elsewhere [21]. Lower temperatures and longer times are also included to verify whether the outgassing mechanism is temperature or time-driven. After bonding, the glass/silicone/wafer stack is cleaned by immersion in HF:HNO_3 1:80 and HF:H_2O 1:20 (clean n.2) prior to a-Si:H(i/n$^+$) deposition on the backside. In standalone samples, an additional deposition of a-Si:H (i/n$^+$) on the frontside of the wafer is performed after clean n.2, since the frontside passivation is removed during the HF:HNO_3 step. Quasi Steady State Photoconductance (QSSPC) [26] and photoluminescence (PL) [27] measurements of the standalone and bonded wafers are taken to evaluate the effective minority carrier lifetime τ_{eff}, while Fourier Transform Infrared Spectroscopy in Attenuated Total

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