Solar Energy Materials & Solar Cells 119 (2013) 12–17

Contents lists available at ScienceDirect

Solar Energy Materials & Solar Cells

journal homepage: www.elsevier.com/locate/solmat

Smoothening intermediate reflecting layer for tandem thin-film silicon solar cells

M. Boccard [a,*], C. Battaglia [a], N. Blondiaux [b], R. Pugin [b], M. Despeisse [a], C. Ballif [a]

[a] Ecole Polytechnique Fédérale de Lausanne (EPFL), Institute of Microengineering (IMT), Photovoltaics and Thin Film Electronics Laboratory, Rue A.-L. Breguet 2, CH-2000 Neuchâtel, Switzerland

[b] Centre Suisse d'Electronique et Microtechnique CSEM SA, Jaquet Droz 1, CH-2000 Neuchâtel, Switzerland

ARTICLE INFO

Available online 28 April 2013

Keywords:
Solar cell
Multi-junction
Planarization
Lacquer

ABSTRACT

We introduce the concept of smoothening intermediate reflecting layers (IRLs) in Micromorph thin-film silicon tandem solar cells in the superstrate configuration. The aim of such structures is not only to provide a selective reflection of light for optimal light management in both sub-cells but also to tune the morphology of the surface on which the microcrystalline silicon bottom cell is grown. This novel type of IRL is shown to enable the use of rough front electrodes with excellent light scattering properties in Micromorph devices without impacting the electrical property of the microcrystalline material. A low-index (1.5), highly transparent and insulating UV-curable lacquer is used as IRL. The electrical contact between both sub-cells is ensured by a partial covering of this lacquer layer: the bottoms of the structure are efficiently filled whereas the tips are unveiled by an etching step. This results in an efficient smoothening of the surface of the top cell, validated by a V_{oc} boost of up to 50 mV compared to a standard IRL. A strong top cell current increase is also shown, with up to 2.3 mA/cm^2 (20% relative) current gain compared to a cell with no IRL. Adjusting the volume of lacquer composing this advanced interlayer enables a fine tuning of its opto-electrical properties. The introduction of a smoothening IRL is shown, with simple calculations, to be a key element towards the obtaining of 13.5% stable-efficiency Micromorph devices using present state-of-the-art single junctions.

1. Introduction

For efficient photovoltaics devices, light absorption has to be maximized and, simultaneously, the conversion losses from photons to electric charges have to be minimized. For thin-film silicon solar cells, light management is mandatory to absorb a significant part of available light in the thin photoactive layers, both in the case of amorphous silicon (*a*-Si:H) and microcrystalline silicon (μc-Si:H) [1–5]. For Micromorph (*a*-Si:H/μc-Si:H tandem) devices, light trapping is necessary for both sub-cells. This is typically achieved by texturing one or both interfaces between silicon and the electrodes [6–8]. However, depositing thin-film silicon layers on textured substrates results in local defective areas (often called cracks) which are detrimental for the electrical performance of the cell as they cause reduced open-circuit voltage (V_{oc}) and fill factor (*FF*) [9–12].

Adequate trade-offs between optical and electrical performances can be found for *a*-Si:H and μc-Si:H single-junction devices, by using adapted morphologies [2,13]. Yet, the requirements in terms of optimal electrode morphology are different for *a*-Si:H and μc-Si:H devices, μc-Si:H devices requiring a smoother surface compared to *a*-Si:H devices. Thus, it is challenge to optimize light management and growth morphology for both top and bottom cells with only the front electrode for Micromorph devices, even though an electrode morphology enabling excellent light trapping for both sub-cells can be obtained [8]. To overcome this limitation, an additional possibility of adapting the morphology is required, which can be done for example with a multi-scale textured electrode architecture [14–18].

Here, we present another route to add a degree of freedom when designing Micromorph devices. We introduce the concept of smoothening interlayer between the *a*-Si:H and μc-Si:H sub-cells, to adapt the morphology of the surface of the top-cell to grow a high-quality bottom-cell absorber layer. We show that this interlayer can also act as an efficient intermediate reflecting layer (IRL), by selectively reflecting part of the visible light back in the top cell, so that ideal matching conditions can be achieved with thin—and therefore more stable—top-cells [19–21]. Combined to a rough electrode that provides light scattering for both sub-cells, this smoothening IRL enables to maintain excellent electrical properties for the μc-Si:H bottom cell. The potential of such architecture is discussed, and we show that this concept paves the road towards 13.5% stable Micromorph devices.

* Corresponding author. Tel.: +41 32 718 33 20; fax: +41 32 718 32 01.
E-mail address: mathieu.boccard@epfl.ch (M. Boccard).

0927-0248/$ - see front matter © 2013 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.solmat.2013.03.040

2. Motivation

For Micromorph devices, the morphology of the surface on which the second sub-cell is grown is determined by the morphology of the substrate (respectively the superstrate) and the growth of the first deposited sub-cell; this first deposited sub-cell is the μc-Si:H bottom cell in the substrate configuration, and the a-Si:H top cell in the superstrate configuration. In the substrate configuration, the concept of asymmetric IRL was introduced to provide the small and sharp features needed to provide an efficient coupling of light in the a-Si:H top cell [22]. This appears necessary since, if such features were included in the electrode morphology, they would (1) be detrimental to the electrical quality of the μc-Si:H cell and (2) be attenuated by the deposition of the μc-Si:H cell, making them inefficient to enhance light coupling in the top cell.

In superstrate configuration, illustrated in Fig. 1, small features (of typical size up to around 200 nm) can be smoothened by depositing the top cell. This enables to design an electrode that provides light trapping in the top cell without damaging the electrical quality of the bottom cell (with however limited light trapping in the bottom-cell). Yet, in the case of larger features, pinching occurs if the features are not smooth enough, resulting in cracks in the bottom sub-cell [19,15]. The large features necessary to an efficient light trapping in the bottom cell have therefore to be designed in a way that the surface on which the μc-Si:H cell will be grown is smooth enough [15].

The approach that we introduce here is to combine a rough electrode, which provides light scattering to both sub-cells, and an advanced IRL to smoothen the surface on which the μc-Si:H sub-cell is grown. Even though planarization is a standard process for microelectronics, it usually includes high temperature steps (over 300 °C) and employs insulating material. On the other hand, to be used as IRL in thin-film silicon solar cells, a (smoothening) IRL should:

1. Allow serial connection of the top and bottom sub-cells.
2. Be transparent: light trapped in the cell will cross this layer several times, so its absorption should be small (typically $< 10\ cm^{-1}$ for 500 nm–1100 nm).
3. Be resistant to the deposition of the bottom cell (vacuum deposition at 200 °C).
4. Not damage the top cell during its fabrication (< 200 °C process).

Amongst the available techniques, we focus on the deposition of a UV-curable lacquer by spin-coating, followed by its partial etching to ensure electrical connection of both sub-cells. A comparison with other techniques to fabricate smoothening IRLs can be found in [23].

3. Experimental details

Micromorph devices were fabricated on flat glass in the superstrate configuration. Both front and back electrodes consist of ZnO grown by low pressure chemical vapor deposition (LPCVD) [24]. Different IRLs are compared, including no IRL, a 50-nm-thick silicon-oxide-based IRL (SOIR) [19], and two smoothening IRLs, with two different smoothening intensities, as described in the following.

The fabrication sequence of a Micromorph cell with such an IRL is sketched in Fig. 2. A thin (10 nm) sputtered ZnO etch-stop layer is first deposited on top of the a-Si:H cell to protect it from the subsequent fabrication steps (Fig. 2, (2)). Then, a lacquer (Ormocer (R)) from Microresist technology, GmbH is spin-coated on top, and UV-cured to form an insulating glass-like layer, of refractive index of 1.5 (Fig. 2 (3)). To adjust the initial thickness of the lacquer, it was diluted in a specific solvent with a 1:15 ratio. After spin-coating the solution, the solvent is evaporated by placing the samples on a hot plate (90 °C for 15 min), and the samples are placed under UV light for 1 h. When following the same procedure, the thickness of the resulting layer on a reference glass is around 150 nm.

As the surface of the a-Si:H top cell is rough, the lacquer preferentially fills the valleys of the morphology, and is thinner on top of the pyramidal tips originating from the ZnO front electrode morphology. To ensure current flow between the top and bottom sub-cells, a partial etching of the insulating lacquer layer in an SF_6–O_2 plasma is then performed (Fig. 2 (4)). By tuning the duration of this plasma etch, the tips can be unveiled whereas some lacquer is preserved in the valleys. The depositions of the μc-Si:H bottom cell and the back electrode finish the cell fabrication (Fig. 2 (5)). Overall, adjustable parameters are the lacquer dilution (to thin the lacquer layer) and the etching time (to partially remove the lacquer). Only the etching time is changed in the following, the shorter the etching, the smoother the surface.

Fig. 3 shows two cross section views (at different locations) of a Micromorph device including a smoothening IRL, with a 3-min-long

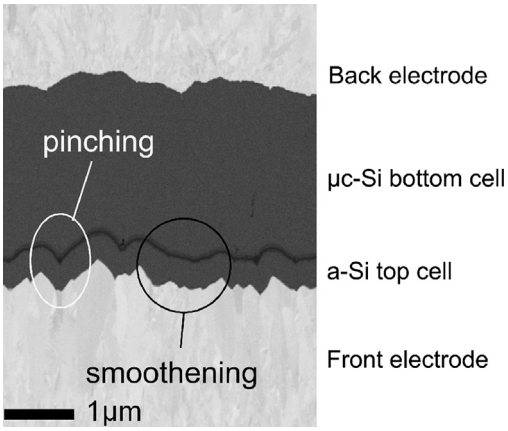

Fig. 1. Cross section of a Micromorph device in the superstrate configuration deposited on a rough ZnO electrode. Pinching and smoothening of the morphology of the front electrode after the deposition of the a-Si:H top cell is illustrated with the white and black ellipses.

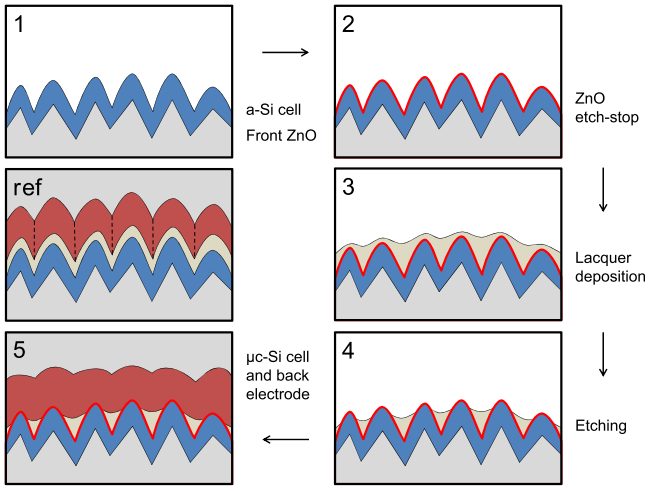

Fig. 2. Schematic view of the processes leading to a Micromorph cell with a smoothening IRL (1–5). A schematic view of a reference Micromorph including a standard IRL is also indicated.