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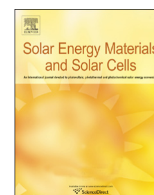

Processed optimization for excellent interface passivation quality of amorphous/crystalline silicon solar cells

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ABSTRACT

This study evaluates the interface passivation quality of the amorphous/crystalline heterointerface and the performance of the heterojunction with intrinsic thin layer solar cells via values of a plasma parameter characterized by the deposition pressure (p) × electrode distance (d). Increasing the product of $p \times d$ leads to a lower crystalline fraction and higher hydrogen content, and enhances the c-Si surface passivation. This $p \times d$ evaluation factor is also compared with other evaluation factors, such as the silane depletion fraction and film-crystallinity. The tendencies of minority carrier lifetimes with respect to these evaluation factors were similar. Using the highest $p \times d$ value of 48, the photovoltaic parameter of the device yielded an open-circuit voltage of up to 710 mV, in turned giving an efficiency of 19.12%.

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1. Introduction

Heterojunction with Intrinsic Thin Layer (HIT) solar cells is currently being researched with great interest, due to their high conversion efficiency, low temperature production processes with lesser chances of device degradation, and better temperature coefficients [1–3]. The key factor for the high performance of the HIT solar cell is the hydrogenated amorphous silicon/crystalline silicon heterointerface, since this interface feature directly affects the junction properties and hence, the solar cell output [4]. However, the deposition conditions strongly effect the structural and physical properties of the thin hydrogenated amorphous silicon (a-Si:H) layer, as well as a-Si:H/crystalline silicon (c-Si) interface. Amorphous silicon can be completely obtained at a low temperature of around 100 °C, while it is believed that an ultra-thin layer grows epitaxially on c-Si surface above this temperature [4,5]. High hydrogen dilution promotes the formation of crystallites even on amorphous substrates such as glass [6]. On c-Si wafers, high hydrogen/silane ratios can lead to epitaxial growth and hence high surface recombination [6]. The unexpected epitaxial-Si (epi-Si) growth on the c-Si wafer is suppressed by using high deposition pressures (p) due to higher deposition rates [4]. Less epi-Si formation on the c-Si at higher p and deposition rates, or a complete lack thereof, was attributed to the use of highly depleted silane plasma [7].

High crystallinity growth contributes to the prejudicial surface passivation effect [8]. Intrinsic rich-hydrogenated-amorphous silicon film is shown, otherwise more disordered, which may lead to lifetime reduction after excessive annealing, which in turn reduces the cell efficiency. Hence, to achieve high open-circuit voltage and efficiency without suffering from thermal degradation, the phase of a-Si:H(i) should push toward the amorphous-crystalline near phase region [9]. It is rather difficult to accurately monitor the a-Si:H phase and heterointerface quality in real-time. Accordingly, only a few methods, including real-time spectroscopic ellipsometry (SE), and the silane depletion fraction (F), have been effective for a-Si:H/c-Si interface diagnosis [4,10]. In this paper, the tendency of the $p \times$ electrode distance (d) product value is investigated for the first time, and is compared with other surface passivation diagnosis techniques, such as the film-crystallinity (X_C), the silane depletion fraction, and then is used as an evaluation factor for optimizing the c-Si surface passivation. Based on this study, heterojunction solar cells with comparatively high performance were fabricated.

2. Experimental methods

The solar cell devices fabricated for this experiment consist of a commercial Czochralski-grown (CZ) Si wafer (1–10 Ω cm, 525-μm thick, ⟨100⟩ oriented), with a specular surface on the front side and

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an unpolished surface on the rear side, treated by a sequence of acetone/methanol/deionized water, and RCA. Immediately before a-Si:H deposition, the native oxide was removed from the wafer by dipping it into 1% hydrofluoric acid for 1 min. The a-Si:H(i) layers were then deposited on both sides of a CZ c-Si wafer, using a $p \times d$ growth product value in the range of 4–48 (Torr × mm), with p and d varied in the range of 0.2–0.8 (Torr) and 20–80 (mm), respectively. A power density of 50 mW/cm^2 at very high frequency (60 Mhz) was used, and the substrate temperature was maintained at 200 °C. The details of the structure and fabrication process of the complete heterojunction solar cells can be found elsewhere [3].

All of the deposited films were measured using SE (VASE®, J. A. Woollam, 240 nm < λ < 1700 nm) at room temperature. The dielectric function, the film thickness, and the film-crystallinity were obtained using the Tauc–Lorentz method combined with the Bruggeman effective medium approximation (BEMA) model. F is defined as $F=(P_o-P)/P_o$, where P_o and P are the silane partial pressure with the plasma turn off, and on, respectively. To measure F during a film deposition, the plasma was first turned on with the required input power, deposition pressure, and electrode distance. Until the plasma stabilized, the silane partial pressure (P) was monitored. The plasma was then turned off, while the computer continued to monitor the P_o. The silane partial pressure in the on and off states was performed with Fourier transform infrared (FTIR) spectroscopy by a single-pass measurement in the exhaust line of the reactor. Further detail on determination of the silane partial pressure by FTIR measurements can be found in Strahm et al. [11]. In order to determine the heterointerface quality, the minority carrier lifetime (τ_{eff}) was measured by the Quasi-Steady-State Photoconductance method, using a commercial photoconductance set-up from Sinton Consulting (WCT-120). The quantum efficiency (QE) of the heterojunction solar cells was measured using a xenon lamp, a monochromator, and optical filters, which filtered out the high orders with a light probe beam impinging normal to the samples. The solar cell performance was characterized by current–voltage measurements under Air Mass 1.5 Global (100 mW/cm^2, AM1.5G) at 25 °C conditions.

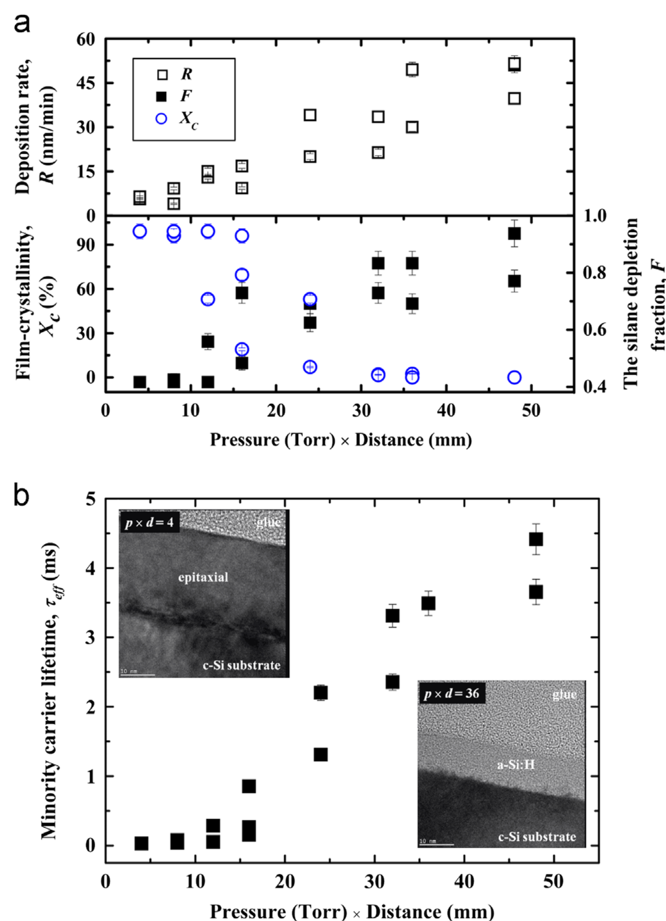

Fig. 1. (a) The film-crystallinity X_c, the silane depletion fraction F, and deposition rate R as a function of $p \times d$ product values. (b) Minority carrier lifetime τ_{eff} as a function of $p \times d$ product values; the inset shows cross-sectional TEM images of a-Si:H(i) deposition on a c-Si wafer for $p \times d$ product values of 4 and 36. Wafers are passivated with 6 ± 1 nm a-Si:H(i) layers.

3. Results and discussion

Fig. 1(a) depicts the crystallinity of the films deposited on the c-Si surface, the silane depletion fraction, and the deposition rate (R) as a function of the $p \times d$ product values. It can be observed that the film-crystallinity reveals trends opposite to those of the silane depletion fraction and deposition rate. As proposed by Strahm et al., the silane depletion fraction value is estimated as following [11].

$$F = \left(1 + \frac{a/kn_e}{[1+c]}\right)^{-1} \quad (1)$$

where kn_e is the silane dissociation frequency, which is related to the radio frequency power and excitation frequency; c is the silane input concentration; and $1/a$ is an effect that essentially correspond to the residence time. Thus, F increases with the product of $p \times d$, because the silane residence time in the reactor increased [11]. This increase of the silane depletion fraction could be the reason for the increasing deposition rate as well [12]. The film-crystallinity clearly decreases with increasing the $p \times d$ product values. Lower $p \times d$ product (as p is lowered or d is decreased) results in the reduction of radical interaction with another gas particle probability, and also shorter the radical distance to reach an electrode as well. The lower radical interaction and shorter radical distance lead to significantly reduce electron density (N_e), but increase the electron temperatures (T_e) [13]. Thus, those radicals first bombard and then stick to crystal sites or give their energy to lower-energy radicals, as in turn, surface diffusion is activated. Both the surface diffusion and sticking of radicals at crystal sites favor crystalline growth [11,14]. Nevertheless at high $p \times d$ product values (increase of p or d), the number of ionization events would be enhanced [13], and in turn, the silicon radicals collide more with similar constituents, which increases N_e and simultaneously reduce the T_e. The increase in N_e, and the decrease in T_e with increasing $p \times d$ product values favors the volume reaction rather than surface reaction, because of the reduction in the mean free path of generated radials in the plasma [12]. This process is also called silicon radical thermalization. The radical thermalization reacts immediately at any site, including non-crystal sites, which may be preferable for amorphous silicon growth [14]. Moreover, it was reported by Zhang et al. that higher deposition rate due to an enhanced number of ionization events with increasing $p \times d$ product values favors the role of silyl radicals in the film growth of relative species such as SiH_2 and H [13]. This higher amount of silyl radicals in the films leads to the transition from crystalline to amorphous phase as the $p \times d$ product values increase. Thus, our results are in accord with those of Fujiwara and Kondo [2], who showed that the film deposition at higher deposition rate could prevent epitaxial growth.

Fig. 1(b) shows the minority carrier lifetimes of passivated c-Si wafers obtained by a-Si:H deposition for different $p \times d$ product values. The τ_{eff} hardly change when the $p \times d$ product value in the range of 0–16. This negligible changing may be due to the presence of high film-crystallinity, which can suppress the c-Si surface passivation [4,8]. A noteworthy improvement of the minority carrier lifetimes is seen with a $p \times d$ product beyond 16. The increase of the τ_{eff} with increasing $p \times d$ product in the range of 16–32 can again be

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