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Data Article

Q1 A novel reversible logic gate and its systematic approach to implement cost-efficient arithmetic logic circuits using QCA

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ABSTRACT

Quantum-dot cellular automata, is an extremely small size and a powerless nanotechnology. It is the possible alternative to current CMOS technology. Reversible QCA logic is the most important issue at present time to reduce power losses. This paper presents a novel reversible logic gate called the F-Gate. It is simplest in design and a powerful technique to implement reversible logic. A systematic approach has been used to implement a novel single layer reversible Full-Adder, Full-Subtractor and a Full Adder–Subtractor using the F-Gate. The proposed Full Adder–Subtractor has achieved significant improvements in terms of overall circuit parameters among the most previously cost-efficient designs that exploit the inevitable nano-level issues to perform arithmetic computing. The proposed designs have been authenticated and simulated using QCADesigner tool ver. 2.0.3.

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Specifications Table

Subject area	*Nanoelectronics*
More specific subject area	*Nanotechnology QCA reversible logic design*
Type of data	*Table, figure*
How data was acquired	*QCADesigner software Bistable engine and Analysis process have been applied to attain the data results*
Data format	*Analyzed*
Experimental factors	*Reversible F-Gate has been proposed. It has been testified to determine various arithmetic logic circuits*
Experimental features	*Computational Simulation study has been used to determine results*
Data accessibility	*Data is available within this article*

Value of the data

- Gates are the basic building block to design logic in digital systems. A new reversible F-Gate has been proposed to enhance the performance of digital systems.
- Adder circuits are widely investigated since their performance can directly affect the whole digital system performance. We have proposed an optimal reversible Arithmetic circuits including Adder, Subtractor and Adder-Subtractor using the proposed F-Gate.
- The presented circuit designs and data analysis can support the researchers to reduce the circuit complexity and implement high robust Arithmetic logic designs.
- The proposed QCA reversible designs can be used to reduce hardware cost and design energy lossless arithmetic logic unit (ALU) in quantum computers.

1. Data

In this paper, a new high speed and a low power reversible gate called the F-Gate has been proposed. The logic symbol, QCA layout, and its simulation results are shown in Fig. 1. The proposed gate has been used in a systematic manner to implement single layer arithmetic logic functions such as reversible Full Adder (RFA), reversible Full Subtractor (RFS) and reversible Full Adder-Subtractor (RFAS). The logic symbol, QCA layout, and simulation results of the proposed Arithmetic circuits are shown in Figs. 2–4, respectively. A detailed report on the hardware costs achieved from the proposed QCA implementations in terms of area, cell counts and clock delays are provided in Table 1. However, the structural evaluation of the proposed RFAS circuit has been compared with their conventional counterparts [1–5]. The detailed comparison results of RFAS are shown in Table 2.

2. Experimental design, materials and methods

QCADesigner tool ver. 2.0.3 [6] with default parameters have been verified the functioning of the proposed QCA-circuits. The default parameters are listed as: QCA cell size = 18 nm, diameter of quantum dots = 5 nm, number of samples = 50,000, convergence tolerance = 0.001, radius of effect = 65 nm relative permittivity = 12.9, clock low = 3.8e−23 J, clock high = 9.8e−22 J, clock amplitude factor = 2.000, layer separation = 11.5 nm and maximum iterations per sample = 100. The simu-

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