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Experimental investigation of microchannel coolers for the high heat flux thermal management of GaN-on-SiC semiconductor devices

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Abstract

Experiments on removing high heat fluxes from GaN-on-SiC semiconductor dies using microchannel coolers are described. The dies contain an AlGaN/GaN heterostructure operated as a direct current resistor, providing a localized heat source. The active dimensions of the heat source are sized to represent the spatially-averaged heat flux that would appear in microwave power amplifiers. A wide variety of microchannel materials and configurations are investigated, allowing a comparison of performance and the resulting GaN temperatures. Silicon and AlN microchannel coolers exhibit good performance at lower power densities (1000–1200 W/cm^2 over 3×5 mm^2 to 2×5 mm^2 active areas). Polycrystalline chemical vapor deposited (CVD) SiC microchannel coolers are found to be extremely promising for higher power densities (3000–4000 W/cm^2 over 1.2×5 mm^2 active areas with 120 °C GaN temperature). A hybrid microchannel cooler consisting of low-cost CVD diamond on polycrystalline CVD SiC exhibits moderately better performance (20–30%) than polycrystalline CVD SiC alone.

Keywords: Microchannel cooler; Single phase flow; Electronic packaging; Diamond

1. Introduction

Wide bandgap semiconductor technology, based around SiC and GaN, has excellent potential for high-power applications, including microwave devices and power switching electronics [1]. This is due to the combination of high electron sheet charge density and saturation velocity, good electron mobility, and in particular, the very high breakdown electric field strength of wide bandgap materials compared to Si, GaAs, and InP semiconductors [1], as listed in Table 1. A device of particular importance for microwave applications is the AlGaN/GaN high electron mobility transistor (HEMT) [2], consisting of a horizontal electrically conducting channel with source, gate, and drain metallizations, as shown in the layout of Fig. 1a. The gate is very short in the x-direction, typically with L_G of 0.5 μm or less. For high power operation, such HEMTs are grown by chemical vapor deposition (CVD) processes on high thermal conductivity, single crystal SiC substrates, typically semi-insulating 4H–SiC or 6H–SiC. In laboratory settings, such HEMTs have produced 5–10 W of microwave power per mm of gate width w (in the y-axis direction), with isolated experiments near 30 W/mm [2,3]. These values are factors of 4–25 above any competing technologies. The dissipated power densities directly under the miniscule gates in the GaN-based HEMTs are incredible, of order 1–2 MW/cm^2, but in test devices with a very modest total gate width ($\leqslant$0.3 mm), the heat easily spreads in a 3D fashion into the substrate and the thermal management problem is not particularly vexing.

However, when one wants to generate much larger total powers by increasing the total gate width, for various technical reasons, it is necessary to use a multi-fingered HEMT layout as shown in Fig. 1b. Briefly, the layout is necessary to avoid signal transmission losses due to distributed gate

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Nomenclature

d	microchannel width (m)
D	microchannel hydraulic diameter (m)
f	friction factor
F_H	heat flux (W/cm^2)
h	heat transfer coefficient (W cm^{-2} K^{-1})
h_{wall}	microchannel wall heat transfer coefficient (W cm^{-2} K^{-1})
L_{active}	length of active region on the die (m)
L_G	transistor gate length (m)
L_p	gate-to-gate pitch spacing (m)
Nu	Nusselt number
Pr	Prandtl number
$P_{W(waste)}$	waste heat dissipated per unit gate width (W/mm)
Re	Reynolds number for microchannel
t	microchannel height (m)
T_B	bulk fluid temperature (°C)
w	transistor gate width (m)

Greek symbols

κ	thermal conductivity of the microchannel cooler material (W m^{-1} K^{-1})
κ_f	thermal conductivity of the fluid (W m^{-1} K^{-1})

Table 1
Properties of semiconductor materials and heterostructures

Material property	Material (heterostructure)				
	Si	GaAs (AlGaAs/InGaAs)	InP (InAlAs/InGaAs)	4 H–SiC	GaN(AlGaN/GaN)
Bandgap (eV)	1.10	1.42	1.35	3.26	3.49
Electron mobility (m^2 V^{-1} s^{-1})	0.15	0.85 (1.0)	0.54 (1.0)	0.070	0.090 (>0.2)
Saturated electron velocity (m/s)	1.0×10^5	1.0×10^5	1.0×10^5	2.0×10^5	1.5×10^5
Electron sheet charge density (m^{-2})	–	4×10^{16}	4×10^{16}	–	$1–2 \times 10^{17}$
Breakdown electric field (MV m^{-1})	30	40	50	200	330
Thermal conductivity (W m^{-1} K^{-1})	150	50	70	450	130–170

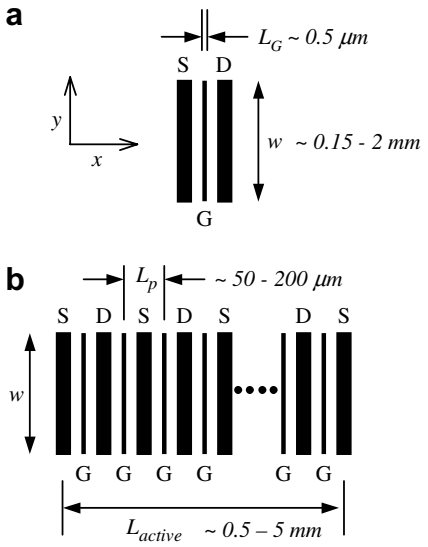

Fig. 1. Top view of transistor layouts, showing (a) single and (b) multi-fingered configurations. Source (S), gate (G), and drain (D) metallizations are indicated. The electrically conducting channel and the underlying substrate die are beneath the metallizations in the plane of the paper.

resistance and gate capacitance that would occur along a single, extremely wide gate, as well as to minimize electromagnetic time delay (phasing) problems. The layout of Fig. 1b also helps conserve expensive substrate area. When one contemplates creating microwave devices and monolithic microwave integrated circuits (MMICs) with total power dissipations of 100 or even 300 W, the dimensions of this "active area" $w \times L_{active}$ enclosing the fingers can become substantial, from several mm^2 to 10 mm^2, depending on the operating frequency. The spatially-averaged power density within the active area [4,5] is the W/mm waste heat dissipation per unit gate width $P_{W(waste)}$, divided by the gate-to-gate pitch spacing L_p in Fig. 1b. So for 5 W/mm $P_{W(waste)}$ and a typical 50 μm pitch, the spatially-averaged power density is 10 kW/cm^2; even for a much more generous 200 μm pitch it is 2.5 kW/cm^2. For a 200 W dissipation device, the relevant areas are 2 and 8 mm^2, for the 50 and 200 μm pitch, respectively.

Removing these levels of total power and heat flux is a challenging problem if a reasonable HEMT gate temperature (150–175 °C) is to be maintained [4,5]. Although still localized, the peak heat fluxes appearing on the rear of a typical 100–380 μm thick substrate die are expected to be several kW/cm^2, so techniques of removing high heat fluxes are of paramount importance. An example of the simulated temperature profiles in the x-direction for a multi-fingered HEMT structure (at 5 W/mm $P_{W(waste)}$ and 50 μm pitch) is shown in Fig. 2, for several different heat transfer coefficients h on the rear of the 380 μm thick die. The ANSYS thermal simulation code (ANSYS Inc., Canonsburg, PA, USA) was used and further details of methodology and geometry are given elsewhere [6]. For each case, two temperature profiles are shown, one is the temperature on