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New FPGA based hardware implementation for JET gamma-ray camera upgrade

A. Fernandes[a,*], R.C. Pereira[a], B. Santos[a], J. Bielecki[b,c], G. Boltruczyk[d], A. Broslawski[d], P.F. Carvalho[a], R. Dias[a], J. Figueiredo[a,c], L. Giacomelli[e], M. Gosk[d], V. Kiptily[c], S. Korolczuk[d], A. Murari[c], M. Nocente[e,f], D. Rigamonti[e,f], J. Sousa[a], M. Tardocchi[e], A. Urban[d], I. Zychor[d], C.M.B.A. Correia[g], B. Gonçalves[a], JET Contributors[1]

[a] Instituto de Plasmas e Fusão Nuclear, Instituto Superior Técnico, Universidade de Lisboa, 1049-001, Lisboa, Portugal
[b] Institute of Nuclear Physics Polish Academy of Sciences, PL-31342, Krakow, Poland
[c] Culham Centre for Fusion Energy, Culham, United Kingdom
[d] Narodowe Centrum Badań Jądrowych (NCBJ), 05-400, Otwock, Poland
[e] Istituto di Fisica del Plasma "P. Caldirola", CNR, Milano, Italy
[f] Dipartimento di Fisica "G. Occhialini", Università degli Studi di Milano-Bicocca, Milano, Italy
[g] LibPhys-UC, Department of Physics, University of Coimbra, P-3004 516, Coimbra, Portugal

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ABSTRACT

The Gamma-Ray Camera Upgrade (GCU) project aims at installing a new set of 19 scintillators with multi-pixel photon counter (MPPC) embedded, capable to meet the high fluxes expected during deuterium-tritium plasmas while improving the diagnostic spectroscopic capabilities. GCU will benefit from the Advanced Telecommunications Computing Architecture (ATCA)-based Data Acquisition System (DAQ), successfully installed and commissioned during the JET-EP2 enhancement. However, to cope with the new GCU detector signals, the DAQ Field Programmable Gate Array (FPGA) codes need to be rebuilt. This work presents the FPGA code upgrade for Gamma Camera (GC) DAQ, capable to sustain the expected fast response of new detectors, while exploiting the full capabilities of the DAQ. Dedicated codes were designed, capable to acquire the new signals at full rate, and simultaneously processing them in real-time through suitable algorithms, fitted to the new signals shape. First results of real-time processing codes applied to data from detector prototypes are presented.

1. Introduction

The 2D Gamma-Ray Camera (GC) of the Joint European Torus (JET) is one of the target diagnostics for physics exploitation during next high-power Deuterium-Tritium (DT) experiments [1]. From the gamma-ray emission spectra, associated with specific reactions among fast ions and fusion alphas with impurities, it will be possible to infer information on the spatial distribution of these fast ions and alpha particles, and to follow their evolution in time [1,2].

The Gamma-Ray Camera Upgrade (GCU) project aims to improve the spectroscopic properties of the existing GC in terms of energy resolution and high counting rate capability, allowing its operation during DT [3,4]. New 19 $LaBr_3$(Ce)-based detectors were installed during 2017 shutdown, featuring an energy resolution of 5% (Energy Resolution = FWHM/Eγ) at 1.1 MeV and count rate capability of 500 kCounts/s [4–6].

The GCU Data Acquisition (DAQ) system, an Advanced Telecommunications Computing Architecture (ATCA)-based DAQ successfully installed and commissioned during the JET-EP2 enhancement [7], aims at acquiring and simultaneously processing the new 19 GCU detector signals. Dedicated algorithms for DAQ Field Programmable Gate Arrays (FPGAs) are being developed, capable of real-time processing the incoming signals, delivering only the energy value of registered events and their corresponding occurrence time. During past experiments the DAQ was operating at a down-sampling rate of 2.5 MSamples/s, coping with the pulse length of former CsI(Tl)-based detectors [7]. Thus, new algorithms are needed to process the new fast signals at full DAQ rate, as described in the next sections.

* Corresponding author.
E-mail address: anaf@ipfn.tecnico.ulisboa.pt (A. Fernandes).
[1] EUROfusion Consortium, JET, Culham Science Centre, Abingdon, OX14 3DB, United Kingdom.

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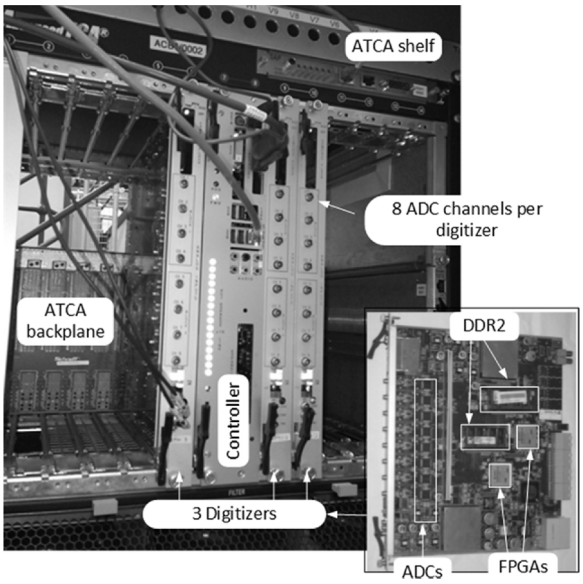

Fig. 1. ATCA-based DAQ system in the GCU cubicle. Main components are highlighted including a top-side picture of the digitizer module.

2. GCU DAQ

The GCU DAQ system, detailed in Fig. 1, is composed of an ATCA shelf with 3 digitizer modules connected to a controller through the ATCA backplane using the PCI-express (PCIe) communication protocol [8]. Each ATCA digitizer module is composed of eight Analog to Digital Converters (ADC) with a maximum sampling rate of 250 MSamples/s, 2 GB of local memory (DDR2) and two Virtex-4 FPGAs (XC4VFX-60-11ff1152) [9].

As detailed in Fig. 2, each FPGA is responsible for the data-path and real-time processing of 4 ADCs data.

For both former and new detector signals, the FPGA code was developed using the HDL (hardware description language) Verilog, benefiting from some Intellectual Property (IP) cores available in the ISE Xilinx Compiler catalog (e.g. Memory controller and PCIe endpoint).

Besides the basic module functionalities (e.g. data path; configurations), the true parallelism of FPGAs make them suitable for real-time processing and data reduction. Four data management operation modes were designed for the GCU FPGAs: i) Raw data – all acquired samples (1 sample = 16-bit) are stored in the local memory; ii) Event storage - events above a predefined threshold are stored (predefined samples to cover the pulse) plus the corresponding time occurrence; iii) Processed data – perform real time analysis and storage of the event energy value plus its time occurrence; iv) filter – when a processing filter is present (e.g. trapezoidal shaper [10]), this option stores filtered data for calibration and debug (no data reduction). For all modes, stored data is sent through PCIe Direct Memory Access (DMA) packets to host when the acquisition finishes.

According with Figs. 3 and 4, events from former CsI(Tl) detectors (Fig. 3) present a much longer decay and a slightly different shape, when compared with new $LaBr_3$(Ce) signals (Fig. 4). The events from CsI(Tl)-based detectors (Fig. 3), in operation until end of 2016, present pulse lengths > 400 us, and shape similar to ramp-like pulses. Filtering algorithms were implemented in the DAQ FPGAs to digitally reduce the pulse size, at a down-sampling rate of 2.5 MSamples/s [11]. The maximum count rate attained with the former detectors was 20 kEvents/s. The expected count rates of 500 kCounts/s during DT [4–6] justifies the detectors replacement.

$LaBr_3$(Ce) detectors deliver short pulses instead with sharp peaks and fast decay (~120 ns pulse length), similar to exponentials (Fig. 4), being capable to sustain the expected count rates during DT

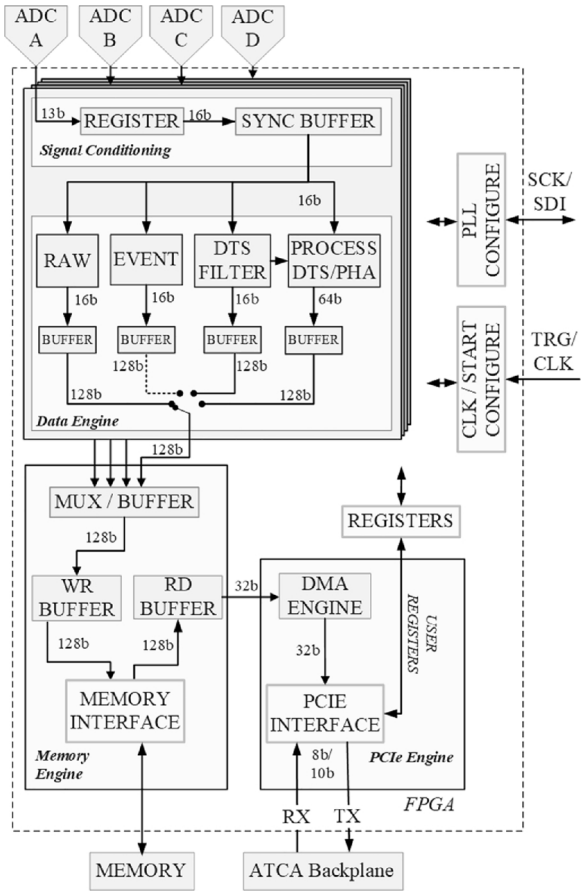

Fig. 2. FPGA code flowchart. Four main blocks highlighted corresponding to: i) the input signal conditioning; ii) operating modes available (data engine); iii) storage/retrieval to/from DDR2 local memories (memory engine); and iii) PCIe interface for read/write requests and DMA transfers (PCIe engine).

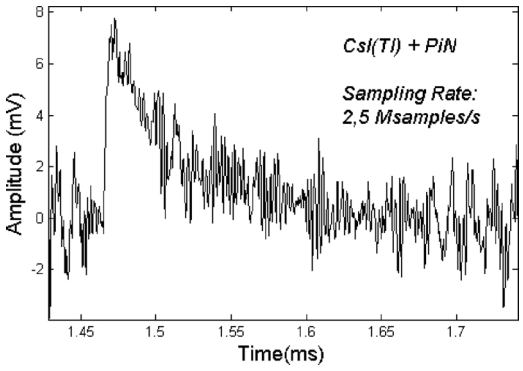

Fig. 3. Event from CsI(Tl)-based detectors acquired at 2.5 MSamples/s, with GC in operation during experiments.

(~500 kEvents/s). New algorithms were identified and implemented at GCU FPGAs, capable to acquire and process the fast $LaBr_3$(Ce) incoming signals at a sampling rate of 200 MSamples/s (maximum sampling rate allowed by the DAQ when all digitizer channels are used).

Considering the maximum local memory available for data storage per discharge (2 GB of DDR2 shared by 4 ADCs −500 MB/ADC), while no data storage restriction existed for the former detectors, operating at a slow rate of 2.5 MSamples/s, constrains are now imposed when operating at 200 MSamples/s and with the foreseen high count rates. Table 1 details the memory needed to store the new detector events (event itself or processed data) during DT considering the maximum expected count rate (Count Rate (kEvent/s)) of 500 kEvents/s during