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Testing results of chopper based integrator prototypes for the ITER magnetics

Antonio J.N. Batista[a,*], Graham Naylor[b], Llorenç Capellà[d], Andre Neto[c], Adam Stephen[b], Nicoletta Petrella[b], Stephanie Hall[b], Jorge Sousa[a], Bernardo Carvalho[a], Filippo Sartori[c], Roberto Campagnolo[c], Isidro Bas[e], Bruno Gonçalves[a], Shakeib Arshad[c], George Vayakis[f], Stefan Simrock[f], Luca Zabeo[f]

[a] *Instituto de Plasmas e Fusão Nuclear, Instituto Superior Técnico, Universidade de Lisboa, 1049-001, Lisboa, Portugal*
[b] *CCFE, Culham Science Centre, Abingdon, Oxon, OX14 3DB, UK*
[c] *Fusion for Energy, Josep Pla 2, 08019, Barcelona, Spain*
[d] *Vitrociset Belgium Sprl, Gravendijckseweg 53, 2201 CZ, Noordwijk, The Netherlands*
[e] *GTD Sistemas de Informacion, 08005, Barcelona, Spain*
[f] *ITER Organization, Route de Vinon-sur-Verdon, CS 90 046, 13067 St. Paul Lez Durance Cedex, France*

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ABSTRACT

Several design variants of chopper-based digital signal integrators have been tested to evaluate the optimal solution to achieve the ITER magnetics diagnostic requirements. A maximum flux-equivalent drift of 500 μ V.s/hour is one of the key ITER magnetics diagnostic constraints for the integrators. The flux drift must be below the specified limit whilst the device satisfies other stringent specifications such as, 500 V galvanic isolation, 14-bit ENOB and environment magnetic field tolerance up to 10 mT. This paper presents the results of some of the tests performed on the integrator prototypes developed. These include tests to verify the integrator drift during long experiments when subjected to different conditions, e.g., imposition of a common mode voltage and input signals with a frequency spectrum that challenges the design limits.

1. Introduction

The ITER magnetics diagnostic will be very important for real-time control of some of the main plasma parameters (e.g. position and shape), as well as being key for investment protection (via an interlock system). Superconducting tokamaks, such as ITER, can sustain plasma discharges for a duration reaching one hour. One of the limiting factors of the magnetics diagnostic arises because it requires measurements to be integrated in time, a process that results in error accumulation. This growing error can ultimately compromise plasma control and can thus limit the achievable plasma duration.

This well-known ‘drift’ problem has been studied for different superconducting machines [1–8]. Two main development branches are evolving, analogue integration and real-time digital integration based on the signal chopping concept. Both approaches have advantages and disadvantages [8].

Real-time digital integration, based on the signal chopping concept, was chosen for the modules tested for ITER.

The presented test results are an extension of the work published in [8], where the architecture of the modules under test, and the test rig used, are described.

2. Tests and results

A total of eight different designs have been developed. For statistical purposes, a batch of four modules was manufactured for each design, accounting for a total of 32 modules. In this work the results of the tests performed with the first four designs are presented. Tests to determine the drift with an input load, the variation of the drift with temperature and zero-flux tests are not discussed, as these were presented in [8]. As stated in [8] Design 2 had consistently worse results with respect to the remaining designs and is therefore not discussed further.

Tests required to verify if the chopper digital integrator is capable of meeting ITER requirements were repeated at least twice for each module. A minimum duration of 20 min for the tests was set as a requirement by F4E, to decrease testing time and data storage. Tests of 20 min do not guarantee that the drift is below the 500 μV.s/hour specified by ITER (since drift variation is not linear) but the results

* Corresponding author.
E-mail address: toquim@ipfn.tecnico.ulisboa.pt (A.J.N. Batista).

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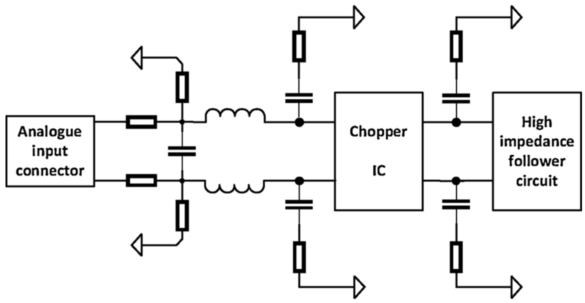

Fig. 1. Module input stage showing the input filter and the snubber circuits before and after the chopper.

extrapolated to one hour are a probable behavior for the modules.

Fig. 1 depicts the module input stage, showing the components before and immediately after the chopper circuit. The input stage components before the chopper are responsible for the Offset Voltage Before Chopper (OVBC), which cannot be compensated by the signal modulation. Conversely, the offset generated by the components after the chopper circuit is automatically removed, to within the design symmetry limits, leaving an acceptably low residual offset, and resulting residual drift, for the considered time-scale. The main differences between designs and between modules of the same design are in Table 1.

Correct measurement of the OVBC is critical to achieve good drift results and at least 10 min were spent to measure it before starting each test, once the modules had warmed up to a stable temperature (This calibration will be also required before each ITER shot).

2.1. Input impedance, common mode current and galvanic isolation tests

The ITER requirement for the module's input impedance is 100 kΩ or above, for a common mode current 0.1 µA or below and with galvanic isolation of at least 500 V. These constraints were met for all designs (the galvanic isolation test was performed with 1 kV).

2.2. Effective number of bits and linearity tests

The ENOB specified value is 14 bits or above for all the Nyquist band. Since the acquisition sampling rate for the tests was 2 MSPS, the minimum sampling rate required by ITER, the Nyquist band is up to 1 MHz.

The ENOB tests were performed without the 10 Hz low pass input filter and with a ± 20 V sine wave up to 200 kHz, which was the maximum output frequency of the low-distortion waveform generator used (SRS DS360). The DS360 has a typical THD of −98 dB at 40 kHz, −88 dB at 100 kHz and −76 dB at 200 kHz.

The attained results differ between designs and modules variations within a design. The ENOB limitation on all modules was the THD value (intrinsic to the design and from the generator for the higher frequency tests).

Design 1 has an ENOB between 15 and 16 bits up to 1 kHz. Above 10 kHz the ENOB is lower than 14 bits (12 bits when the chopper MAX4635 is used).

Design 3 has an ENOB between 15 and 16 bits up to 200 kHz, but this design includes snubbers circuits before and after the chopper that attenuate the signal, putting the respective amplitude far away from the power supply voltage rail limits.

Design 4 has the same behavior as design 3 for the modules with snubbers circuits. For the modules without snubbers it has an ENOB between 15 and 16 bits up to 10 kHz and between 13 and 14 bits above 100 kHz.

Linearity tests were performed on all designs showing very good linearity, with Designs 3 and 4 having a coefficient of determination $r^2 = 0.9999999$ and Design 1 having $r^2 = 0.9999962$ (the linearity test were performed with the help of high accuracy measurements from the multimeter Tektronix DMM4040).

2.3. Zero flux variation test when exposing the modules to a 10 mT magnetic field

In this test a sensor coil was connected directly to the module's differential inputs. The modules under test during experiments were inside a magnetic cage, with a 10 mT steady DC magnetic field (Fig. 2). Each module was exposed to six different magnetic field orientations. During the test a permanent magnet was inserted in, and after 15 min removed from, the sensor coil.

The OVBC was measured during 10 min, with the magnet far away from the coil, and after an initial warm up also of 10 min.

Fig. 3 shows the integrated signal from the sensor coil for designs 1, 3 and 4. Fig. 4 contains a zoom of Fig. 3 when the magnetic flux returns to zero, i.e. at the end of the experiment. From Fig. 4 the drift is below 167 µV.s for the 20 min test, thus the drift values extrapolated to one hour are below the 500 µV.s/hour specified for ITER.

This test also demonstrates that the tested modules withstand an ambient magnetic field of at least 10 mT, as required for ITER.

The dissimilar values for the pulse tops of the integrated signals (Fig. 3) are due to the differences between designs and modules (namely input dynamic range and presence or absence of snubber circuits).

2.4. Zero flux variation test when applying a chirp signal

The test consisted of a sensor coil connected directly to the module's differential inputs. During the test a permanent magnet was inserted in, and after 15 min removed from, the sensor coil. Simultaneously, a chirp signal was applied using an auxiliary excitation coil (Fig. 5).

After an initial warm up of 10 min. OVBC was measured during 10 min, with the magnet far away from the sensor coil and the

Table 1
Main differences between designs and between modules of the same design.

Design	Module	Chopper IC	Snubbers	Anti-aliasing filter IC	ADC
1	1	TS5A23157DGS	no	AD8139ARDZ	AD7960BCPZ (SAR)
1	2	MAX4635EUB	no	AD8139ARDZ	AD7960BCPZ (SAR)
1	3	TS5A23157DGS	no	AD8139ARDZ	AD7960BCPZ (SAR)
1	4	MAX4635EUB	no	AD8139ARDZ	AD7960BCPZ (SAR)
3	1	TS5A23157DGS	yes	LMP8350MA	ADS1675IPAG (ΔS)
3	2	MAX4635EUB	yes	LMP8350MA	ADS1675IPAG (ΔΣ)
3	3	TS5A23157DGS	yes	LMP8350MA	ADS1675IPAG (ΔΣ)
3	4	MAX4635EUB	yes	LMP8350MA	ADS1675IPAG (ΔΣ)
4	1	DG636EQ	yes	LMP8350MA	ADS1675IPAG (ΔΣ)
4	2	DG636EQ	no	LMP8350MA	ADS1675IPAG (ΔΣ)
4	3	DG636EQ	yes	LMP8350MA	ADS1675IPAG (ΔΣ)
4	4	DG636EQ	no	LMP8350MA	ADS1675IPAG (ΔΣ)