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Progress in the development of the EAST timing synchronization system upgrade based on precision time protocol

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ABSTRACT

The timing synchronization system (TSS) plays an important role in the experiments of the Experimental Advanced Superconducting Tokamak (EAST). The purpose of this system is to synchronize each subsystem of EAST according to the reference clock and delay trigger signal, and ensuring stable operation of the EAST fusion device. A prototype TSS module based on precision time protocol (PTP) has been developed using the PXI bus standard and FPGA devices. This new TSS can provide reference clock signals with frequency of up to 50 MHz with isolation fan-out devices. The maximum trigger skewing between different nodes is less than 10 ns. This new TSS is more expandable and suitable for the synchronization and timing control of the EAST fusion experiment. It has been in steady operation since the 2016 EAST experimental campaign. This paper concentrates on the modifications of the TSS, the details about the system architecture and test results will be described in this manuscript.

1. Introduction

The Experimental Advanced Superconducting Tokamak (EAST) has fully superconducting tokamak with a non-circle cross-section of the vacuum vessel and the active cooling plasma-facing components [1]. This key national project consists of many subsystems which are spread out over relatively large distances that need to be synchronized by a synchronization control mechanism to maintain the stable operation of the fusion device.

The former distributed synchronization and timing system (DSTS) on the EAST was based on a set of synchronized optical network which was made up of several pairs of multi-mode fibers. All the nodes distributed in experimental area were connected by these same-length fibers [2]. The accuracy of the system synchronization depended on the difference in fiber lengths among timing nodes, and each node's delay time hinged on the route of the fiber. Therefore it's difficult for maintainers to add new timing nodes to meet the ever increasing demands of the experiments. The motivation for this system upgrade is to set up a stable timing synchronization system (TSS) that is also easy to expand, and convenient to maintain. The new system should provide reference clock signals with frequency of up to 50 MHz, and the synchronization accuracy between different nodes should be in sub-microsecond range.

At present, the most accurate way to synchronize the distributed data acquisition systems is to use the precision time protocol (PTP) IEEE 1588 2008 standard. The protocol is adopted by the EAST CODAC (Control, Data Access and Communication) system to implement the upgraded TSS prototype node. All the nodes with PTP in different places have access to the timing network by normal Ethernet cable, and the timing module on each chassis is synchronized with other IEEE 1588 devices on the network. This paper is organized as follows: the knowledge of PTP is described in Section 2; the structure and the realization of the TSS are presented in Section 3; the application results are shown in Section 4; and finally, the summary is given in Section 5.

2. IEEE 1588 technology overview

IEEE 1588 enables heterogeneous systems that include clocks of various inherent precision, resolution, and stability to synchronize to a grandmaster clock. It supports system-wide synchronization accuracy in the sub-microsecond range with minimal network and local clock computing resources. The protocol has features to address applications where redundancy and security are a requirement [3]. IEEE 1588 defines a special "clock synchronization" procedure [4]. The message exchange of PTP is illustrated in Fig. 1.

The master clock initiates offset correction using "sync" and "follow-up" messages. When the master sends a sync message, the slave uses its local clock to timestamp the arrival of the sync message and compares it to the actual sync transmission timestamp in the master clock's follow-up message. The difference between the two timestamps represents the offset of the slave plus the message transmission delay.

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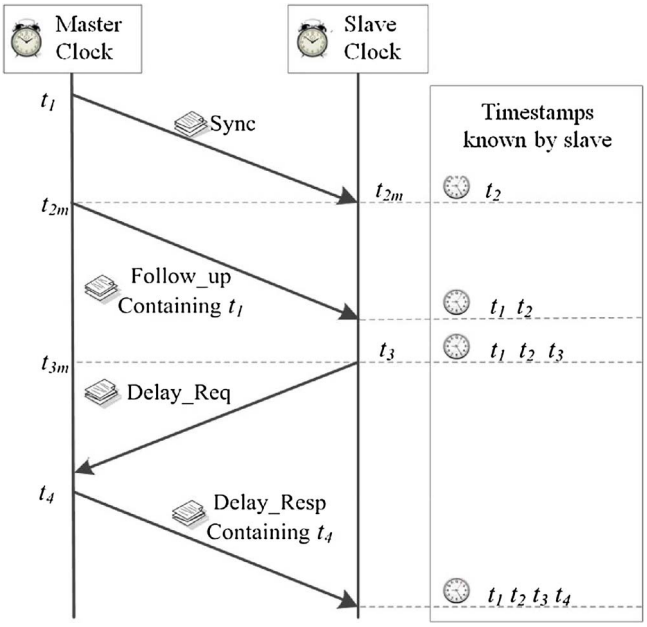

Fig. 1. Messages exchange of PTP.

The slave clock then adjusts the local clock by this difference. To correct for the message transmission delay, the slave uses a second set of sync and follow-up messages with its corrected clock to calculate the master-to-slave delay. The second set of messages is necessary to account for variations in network delays. The slave then timestamps the sending of a delay request message. The master clock timestamps the arrival of the delay request message. It then sends a delay response message with the delay request arrival timestamp. The difference between the time-stamps is the slave-to-master delay. The slave averages the two directional delays and then adjusts the clock by the delay to synchronize the two clocks. Because the master and slave clocks drift independently, periodically repeating offset correction and delay correction keeps the clocks synchronized [5]. The slave clock can get the offset and delay from Eqs. (1) and (2).

$$offset = \frac{t_2 - t_1 - t_4 + t_3}{2} = \frac{(t_2 + t_3) - (t_4 + t_1)}{2} \quad (1)$$

Table 1
The trigger signal properties and functions.

Property	Function
Node Number	Queries and retrievals signal in a small range
Channel Number	Describes the signal location in each node
Signal Name	Describes the main function of each channel
Delay Time	Sets delay time for each trigger channel with 1 ms step
Pulse Width	Sets pulse width for each channel with 1 ms step
Signal Polarity	Sets the signal polarity, such as positive or negative
Channel Enable	Offers the option of enabling trigger
Belonging Subsystem	Describes the destination subsystem that receives the signal

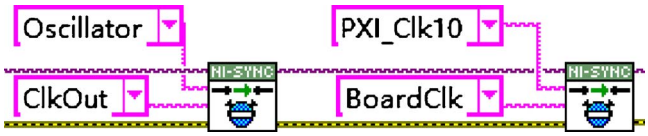

Fig. 3. Block diagram of routing.

$$MSDelay = \frac{t_2 - t_1 + t_4 - t_3}{2} = \frac{(t_2 + t_4) - (t_1 + t_3)}{2} \quad (2)$$

IEEE 1588 message timestamp is the basic factor for IEEE 1588 technology. Ethernet transceiver IC and PHY chips which support timestamp mark are often used to develop in-house devices. In this prototype system, NI PXI-6683 series synchronization boards are used to exchange the PTP messages.

3. System architecture

The upgraded TSS inherits the former console host and database server, optimizes the isolation fan-out modules, and constructs a set of PTP network. The structure of the TSS with two slave nodes is illustrated in detail in Fig. 2.

The master node (MN) and two slave nodes (SNs) are all based on the PXI platform. The MN and SNs are connected by the PTP network. When a system is initialized, the node which receives the GPS signal is defined as the master node as mandated by the software process. All other clocks become slaves and synchronize their clocks with the master. Each node's reference clock is routed to the chassis' backplane, so that all the nodes share the same synchronization time base. The

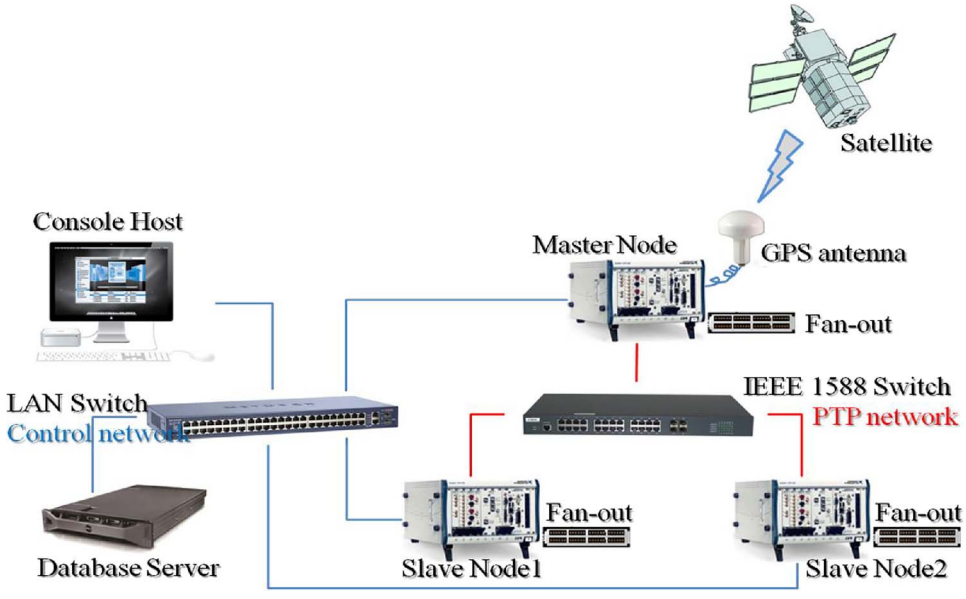

Fig. 2. Structure of upgraded TSS.