

Contents lists available at ScienceDirect

Fusion Engineering and Design

journal homepage: www.elsevier.com/locate/fusengdes



EPICS data acquisition system for FPGA-based plasma electron density measurement on KSTAR



Taegu Lee*, Myungkyu Kim, Woongryol Lee, Giil Kwon, Taehyun Tak, Junewoo Juhn, Jaesic Hong

National Fusion Research Institute (NFRI), Republic of Korea

ARTICLE INFO

Keywords: KSTAR EPICS Channel access (CA)

ABSTRACT

The Korea Superconducting Tokamak Advanced Research (KSTAR) has several diagnostics devices, including a millimeter-wave interferometer (MMWI), far-infrared interferometer (FIR), two-color interferometer, etc., for measuring plasma electron densities. The MMWI diagnostic device measures the electron density of the plasma from the phase difference generated by transmitting a 1 mm (280 GHz) electromagnetic wave into it. The FIR device is similar to the MMWI, but uses a far-infrared (119 um) laser as its electromagnetic wave source. The MMWI is the primary plasma density measurement system in KSTAR. However, its signal contains significant noise and hundreds of fringe-jump events from the phase comparator circuit. The original analogue circuit of the phase comparator is limited in noise handling since it needs to average the raw IF signal to be treated in analogue circuit with limited bandwidth. To handle noise with more flexibility and to reduce occurrence of fringe-jump errors, we developed a new data acquisition (DAQ) system using a high-speed FPGA-based digitizer. The MMWI signal resembles a 10 MHz sine wave. We acquired data at 100 MSPS using a new digitizer. The phase difference per sample was 36°, which lead to inaccurate results due to noise. To increase the accuracy, the new DAQ system has interpolation logic within the FPGA that increases the phase resolution. In addition, the phase comparative value is transmitted to two channels by inverting the signal. The signal that does not travel through the plasma has a phase difference of 180°. The FPGA-based system was constructed using the same algorithm as existing phase comparator circuit [2]. The detected phase was averaged to obtain a phase value, and the result was transmitted as 1280 phase values per msec. In the EPICS Input/Output Controller (IOC), the density is calculated using data received from the direct memory access (DMA) via peripheral component interconnect (PCI) Express, The above FPGA logic was successfully used for real-time feedback control in the ITER CODAC environment. This paper introduces a new, detailed MMWI DAQ system design concept using FPGA, and its operational results.

1. Introduction

The Korea Superconducting Tokamak Advanced Research (KSTAR) includes various diagnostic devices that measure plasma electron density, including the millimeter-wave interferometer (MMWI) [1] system that has been used since the beginning of the KSTAR experiment, the recently introduced FIR device, and the TCI [2] device that has recently undergone installation testing. Each plasma electron density measuring device has different performance characteristics, advantages, and disadvantages. An MMWI diagnostic device is cheaper to construct and easier to maintain than FIR and TCI devices.

However the MMWI does not provide accurate measurements in plasma H-mode due to the presence of fringe-jump events. It is difficult to maintain FIR and TCI diagnostic devices, but they measure plasma electron densities with few errors, even in H-mode. In 2016, an FPGA-based DAQ system was constructed in KSTAR to improve the noise and fringe jump errors in the MMWI diagnostic data and further apply FIR and TCI data [3]. The DAQ system has been used in its current form since the early plasma work in 2008. The new FPGA-based DAQ system was built using a high-speed digitizer in the MTCA.4 open-standard architecture form-factor. The KSTAR is gradually replacing the DAQ system by selecting the MTCA form-factor for ease of maintenance and development of the diagnostic device measurement system. The MMWI diagnostic signal, which has been used since 2008, measures the plasma density using two 5 V probes and reference signals from the phase comparator circuit. However, the new input signal to be provided contains approximately $10\,\mathrm{MHz} + / - 1\,\mathrm{Vpp}$ from the microwave shielding box. This is the signal provided before input to the phase

E-mail address: glory@nfri.re.kr (T. Lee).

^{*} Corresponding author.

comparator circuit. Eventually, we hope to use the MTCA.4 FPGA to improve performance to the point that we can replace the existing phase comparator circuit. In the host computer, the final plasma electron density is calculated using the data acquired via the 100 MSPS digitizer, FPGA logic, and DMA. The FPGA logic IP developed to replace the phase comparator circuit was successfully used for real-time feedback control in the ITER CODAC environment [4–7]. In this paper, we describe the real-time control results with regard to the newly constructed MMWI system and the ITER CODAC evaluation demo.

2. FPGA-based MMWI DAQ system

2.1. FPGA logic for the phase comparator circuit

The new DAQ system was built to determine plasma electron densities using an FPGA, VHDL code, instead of the existing MMWI phase comparator circuit device (multi-fringe counting phase comparator (MFPC)). Thus, the KSTAR MMWI diagnostic device was modified to transmit eight data signals of intermediate frequency (IF), which was down-converted to 10 MHz in a microwave shielding box. Of these eight signals, two reference and probe signals were input into the 100 MSPS FPGA digitizer system, which replaces the phase comparator box in the existing MMWI system. The figure below shows a schematic of the microwave shielding box and the phase comparator of the KSTAR MMWI system [1] (Fig. 1).

Fig. 2 communicates the concept of measuring the phase difference by using the 10 MHz probe and reference signals to obtain the plasma density. The phases of the two channels were compared using the zero-crossing time as the reference point.

FPGA logic was developed based on the above method. The above FPGA logic for the plasma density measurement was completed by using the Python simulation program. However, the KSTAR MMWI diagnostic signal did not exhibit the ideal signal pattern displayed above but rather included noise and more frequency fluctuations than expected. Therefore, additional logic was added as described below. The resulting FPGA logic derives the phase difference values between the two channels of data transmitted through the FPGA; a phase difference of 180 ° is created by inverting the signal that is not transmitted through the plasma.

The system was designed using the same algorithm as the existing MMWI.

The FPGA program logical phase detection schematic functions are listed below:

• Low pass filter (LPF) – allows only signals under 14 MHz (using the finite impulse response filter (FIR)).

- Period lock check checks phase difference over 2
- Oversample data generator increases the resolution of the detected phase from 36 to 9° (4 oversample function).
- Zero cross point detect determines the point in time when the sine waveform changes from negative to positive.
- Phase compare detects a phase difference and the cycle of the current waveform (frequency estimate).
- Degree convert converts to an angle in units of 1 MHz within the range of 6–14 MHz.
- Phase average averages eight phases from oversampled data.
- Period flag gen generates a flag signal to periodically transmit the processed result to the software. Generates 1280 phase signals for each channel per 1 msec.

The angular value of the detected phase difference is transmitted to the S/W of the host PC via the PCI Express DMA shown in Fig. 3. The host PC derives the final plasma electron density using the above values

2.2. DAQ hardware configuration

The MicroTCA.4-form factor digitizer was selected as the new FPGA based DAQ system. The H/W specifications of the new MMWI DAQ system are described below (Table 1).

2.3. Software of plasma electron density calculation

The EPICS IOC [9] was built on the host PC using a standard software framework (SFW) composed of an EPICS library [10]. The phase data includes transmission of 1280 data points per msec to the host PC via the DMA from the FPGA logic. The host PC calculates the density using two-phase data. The plasma electron density was calculated as an average of 20 raw signals by reducing the noise. The electron density calculation method on the host PC was the same as that of the existing DAQ system [11]. The 1280 phase data are stored in MDSplus DB as raw data for plasma density calculation [12].

The two raw data streams and density data are displayed in realtime using Qt OPI panels. The OPI panels were developed using inhouse KWT. The data archive is stored on a local SSD during the process, and then archived to central storage afterwards [13] (Fig. 4).

3. Using FPGA logic for real-time control

This demonstration is intended to verify the CODAC technologies by executing experiments on a real target at a running tokamak (i.e., by controlling real-time plasma density feedback at KSTAR) [4–7].

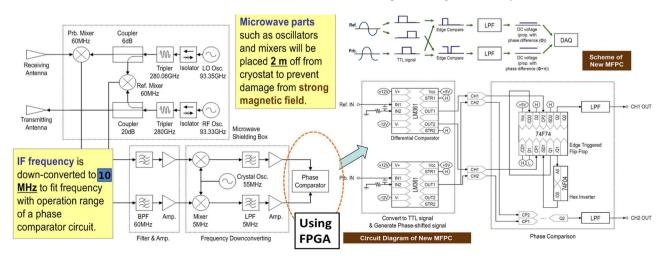


Fig. 1. Schematic of the conventional phase comparator circuit [1].

Download English Version:

https://daneshyari.com/en/article/6743558

Download Persian Version:

https://daneshyari.com/article/6743558

<u>Daneshyari.com</u>