



# A fiber-optic analog isolator of up to 10 MHz bandwidth

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## ABSTRACT

The electromagnetic interference (EMI) around the Experimental Advanced Superconducting Tokamak (EAST) device is very harsh during plasma discharge experiment. In order to reduce the effect of EMI and enhance signal to noise ratio (SNR), a fiber-optic high speed isolator has been designed. Each channel of the isolator has a transmitter unit connected via fiber-optic cable to the receiver unit. A transmitter unit which consists of a 6th order Bessel low-pass anti-aliasing filter, an analog-to-digital converter (ADC), a Field Programmable Gate Array (FPGA), a serializer and an optical transceiver, while a receiver unit comprises an optical transceiver, a deserializer, a FPGA, a digital-to-analog converter (DAC) and a 6th order Bessel low-pass filter. Data from the ADC is serialized by the serializer using 8b/10b encoding before transmission, and 10b/8b decoding was used by the deserializer in the receiver unit. A prototype of this isolator has been realized and tested. The test results show that the transmission bandwidth of analog signal is up to 10 MHz, the transmission delay is typically 500 ns, the transmission distance is up to 250 m and the output noise is less than 5 mV, which can meet the requirements of EAST experimental campaigns.

## 1. Introduction

The Experimental Advanced Superconducting Tokamak (EAST) is a fully superconducting tokamak which comprises 16 D-shaped toroidal field coils, 14 poloidal field coils and its central magnet field is 3.5T [1]. There are also some internal coils and many heating systems, such as the lower hybrid current drive (LHCD) system, ion cyclotron range of frequency (ICRF) system and neutral beam injection (NBI) system, and the total heating power is over 30 MW [2]. These systems can generate high current or high voltage, which may cause electromagnetic interference (EMI). In such a harsh electromagnetic environment, some instruments may not work normally [3]. For example, when the ICRF started working, some signals of the quench detecting system [4] on EAST got offset voltages sometimes, which caused false operation. The interference reason is that the signals of the quench detecting system is transmitted by 60 m electric cables, which were disturbed by the ICRF.

In fact, most of the EMI on EAST is caused by long electric cables. The electric cable likes an antenna, which can easily pick up noise. Some kind of picked up noises have low frequency, which may be less than the frequency of useful signals, so it is hard to use low pass filters to reject them. The signal attenuation also should be taken into account, especially the high speed signals. While the fiber-optic link will not pick up any noises and has no signal attenuation, so it is an ideal solution of long distance transmission (dozens of meters or even more).

Besides, there are many high voltage devices around EAST, such as

NBI system, ICRF system, poloidal field power system and so on. It is dangerous to transmit signals through electric cables from these systems to other ones, while it is quite safe to use the fiber-optic link.

EAST has thousands of signals from several Hz to dozens of MHz or even more [5,6]. The development of the high speed analog isolator via fiber-optic links is quite useful, which can be used as a long distance signal transmission system for high voltage and EMI environments.

There are two principal ways of transmitting analog signals via fiber-optic links, one is using analog digital converter (ADC) [7], and another is voltage frequency converter (VFC) [8]. VFC chip such as AD652 has low clock frequency, which limits the bandwidth of the analog signals (less than 100 kHz), while ADC is a common way to realize high speed analog signal transmission (up to dozens of MHz).

In this article, the high speed ADC and DAC and optical transceivers and FPGAs have been used to realize the fiber-optic analog isolator of up to 10 MHz bandwidth, and the test and measurement analysis have been demonstrated.

## 2. Design

### 2.1. Architecture

The architecture diagram of the fiber-optic analog isolator is shown in Fig. 1. Each channel of the isolator has a transmitter unit connected via fiber-optic cable to the receiver unit. A transmitter unit consists of a

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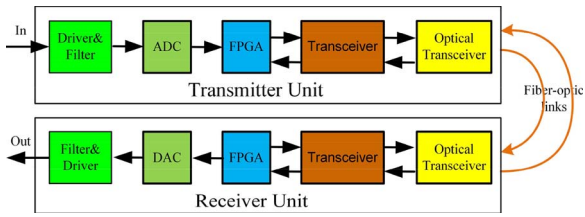


Fig. 1. Architecture of the fiber-optic analog isolator.

**Table 1**  
The configuration of the analog isolator

| Name                | Model       | Description                                                            |
|---------------------|-------------|------------------------------------------------------------------------|
| ADC                 | AD9444      | 80 MSPS, 14-bit, 2 V <sub>pp</sub> differential full-scale input [9]   |
| FPGA                | EP2C5Q208C8 | Cyclone II, 4608 LEs, 119,808 RAM bits, 3 PLLs [10]                    |
| TRANSCEIVER         | TLK1501     | 0.6 to 1.5 Gbps serializer/deserializer, 8b/10b encoding/decoding [11] |
| OPTICAL TRANSCEIVER | AFBR-5921   | 2.125 Gbps, 0.5–300 m link length with 50/125 um MMF [12]              |
| DAC                 | AD9755      | 300 MSPS, 14-bit, 2–20 mA differential output current [13]             |

low-pass filter, an ADC, a FPGA, a transceiver used as a serializer and an optical transceiver, while a receiver unit comprises an optical transceiver, a transceiver used as a deserializer, a FPGA, a DAC and a low-pass filter. Data from the ADC is processed by the FPGA and serialized by the serializer using an encoding technology before transmission, and data check is done by FPGA and a decoding technology was used by the deserializer in the receiver unit.

As this is a very high speed analog isolator, the appropriate chips should be selected for the design. For example, the bandwidth of the isolator is 10 MHz, it's better to choose an ADC of more than 50 MSPS, which is good for signal recovery. Table 1 shows the main configuration of this analog isolator.

## 2.2. Signal conditioning

In the input driver and filter, the AD8138 [14] is easily used as single-ended-to-differential amplifier, whose  $-3$  dB bandwidth is 320 MHz and low harmonic distortion makes it an ideal ADC driver. The common mode voltage is 3.5 V to be compatible with ADC AD9444. The following is a 6th order Bessel low-pass anti-aliasing filter, whose  $-3$  dB bandwidth is about 15 MHz. The input driver and filter is shown in Fig. 2.

In the output filter and driver, R1 is used as current-to-voltage conversion for the output of the DAC AD9755 is current. A 6th order Bessel low-pass filter follows R1 to reduce the output noise, whose  $-3$  dB bandwidth is about 15 MHz. Then the operational amplifier AD8047 [15] is used as differential-to-single-ended amplifier and output driver, whose  $-3$  dB bandwidth is 250 MHz. The output filter and driver is shown in Fig. 3.

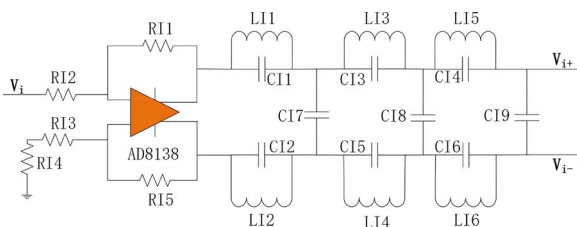


Fig. 2. The input driver and filter.

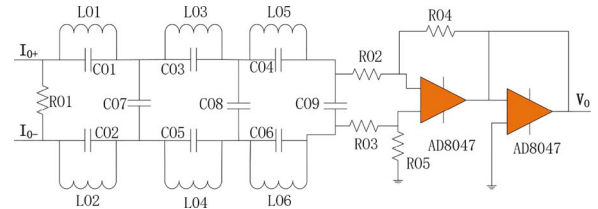


Fig. 3. The output filter and driver.

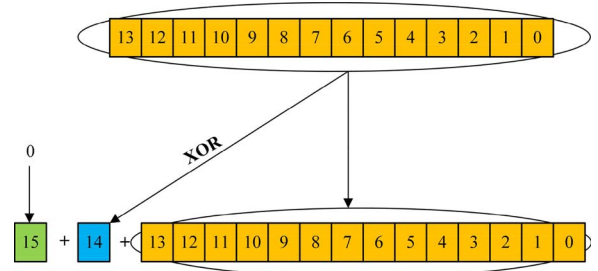


Fig. 4. Algorithm of signal transforms.

## 2.3. Data processing

In the transmitter unit, Data from the ADC is 14-bit, from bit0 to bit13. In order to ensure data integrity, a parity (even) bit is added in processing data by the FPGA as shown in Fig. 4 before data is transferred to the serializer.

$$\text{bit14} = \text{bit0} \oplus \text{bit1} \oplus \dots \oplus \text{bit13}$$

$$\text{bit15} = 0$$

In the receiver unit, after deserializing correct parity is checked by the FPGA.

$$\text{bitck} = \text{bit0} \oplus \text{bit1} \oplus \dots \oplus \text{bit13}$$

If  $\text{bit14} = \text{bitck}$ , then the transmission is fine, else a transmission error occurs, and if the total times of transmission error comes to 5, then the transmission will be aborted and an alarm led will light up.

The 8b/10b encoding technology is used by the serializer in the transmitter unit and the 10b/8b decoding technology is used by the deserializer in the receiver unit to solve the problem of DC balance and recover the data.

## 2.4. Power integrity and signal integrity

As this is a high speed circuit design, the power integrity and signal integrity needs more attention.

The ripple of the digital power is less than 35 mV by LC filters, and the ripple of the analog power is less than 1 mV by the high power supply rejection ratio (PSRR) low dropout regulator (LDO) with good decoupling and routing on PCBs. There are several kinds of LDOs, such as LP38798 for +3.3 V analog power supply of ADC and DAC, TPS7A4901 for +5 V analog power supply and TPS7A3001 for  $-5$  V analog power supply.

Good segmentation of digital ground and analog ground is necessary. Fig. 5 shows an ADC PCB board, in which the ground is segmented into input a power ground, a digital ground, an analog ground and especially an analog ground for ADC.

The system clock is 75 MHz single-ended, which may cause serious radiation, and the differential signal is up to 1.5 Gbps, which may easily cause crosstalk. The following aspects need to be concerned.

- Good routing and good impedance matching (50  $\Omega$ ) and grounding for single-ended signals.
- Good impedance matching and the same routing length for

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