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Temperature calibration and electrical characterization of the differential scanning calorimeter chip UFS1 for the Mettler-Toledo Flash DSC 1

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ABSTRACT

This paper reports on the temperature calibration and electrical characterization of the calorimeter chip UFS1 (internal design XI-400) developed for the new commercially available differential scanning calorimeter (DSC), the Flash DSC 1 of Mettler-Toledo. The chip consists of 2 identical membranes both with a p-type polysilicon microheater in the center of the membrane and a p/n-type polysilicon thermopile for measuring the sample temperature. The temperature calibration of the XI-400 is performed in the temperature range from 208 K to 723 K. An isothermal calibration is first performed to calibrate the heater resistance and the obtained curve is used to calibrate the integrated thermopile. The accuracy of the calibration is then determined by measuring the extrapolated onset temperature (T_e) of primary standards. A detailed electrical characterization of the device is also reported. The calibration method implemented and the good temperature reproducibility of the device allow to use devices with uncalibrated heater resistance in the temperature range from 208 K to 723 K with a typical maximum error of ±5 K.

1. Introduction

Calorimeter chips have became widely used to study thermal properties of sub-microgram samples as function of temperature. They are powerful tools as the small addenda of the calorimetric cell enable to study small amounts of material [1,2]. Ultra-fast-scanning calorimeters are commercially available and extensive characterizations are present in the literature [3–5]. These chips give new possibilities especially for studying the phase transitions of polymers. Scan rates as fast as 1 kK/s prevent recrystallization of the sample during the scan and thermal properties of polymers can be studied under the same conditions as during injection moulding [6–8]. Different designs of calorimeter chips have been proposed with the intent to come to a device capable of fast temperature scan rates [3,9,10]. A common way to achieve this purpose is to reduce the thermal resistance of the calorimeter chip. In this paper an electrical characterization of device XI-400 is carried out to determine its capability in terms of heating and cooling scan rate. Not only the scan rate but also the accuracy of the temperature read out at which a thermodynamic phenomenon occurs is of importance during a calorimetric measurement. The calorimeter chips have to be calibrated in order to establish the relation between the measured signals and the sample temperatures. A common method to calibrate calorimeter chips is with primary standards of which the phase transitions are often fixed or defined ITS-90 points. The output of the chip temperature sensor (i.e. the thermopile output voltage for XI-400) measured for the phase transition of the primary standard is associated directly with the corresponding temperature value present in the literature. Different primary standards can be chosen to cover the entire temperature range of interest. The drawback is that for each primary standard, so for each measured temperature, a different chip has to be used [11] since the sample has to be deposited directly on the chip. Moreover, since the chips used for the calibration are contaminated, calorimetric measurements can be performed only with uncalibrated devices. Techniques based on the use of IR camera are not accurate because it is possible to detect only the incoming radiation power intensity and not the temperature itself. The temperature can be calculated if the emissivity ε of the specimen is known, which is source of large uncertainty [17,18]. In [12] a calibration method that allows the use of calibrated devices for calorimetric measurements is proposed. First the chip is inserted into an oven and the heater integrated on the calorimeter chip is calibrated in the temperature range of inter-

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est. Then the obtained calibration curve is used for the calibration of the temperature sensor, i.e. the thermopile. In this paper the chip XI-400 has been calibrated according to the method presented in [12] for temperatures ranging from 208 K to 608 K. In order to determine the accuracy of the calibration the T_e of primary standards has been measured with chips having uncalibrated heater resistance. The primary standards have been chosen so that their phase transition is inside the temperature range from 208 K to 723 K. In the first part of the paper the main characteristics of the chip XI-400 are briefly outlined. A detailed electrical characterization of the chip follows. In the last part of the paper the temperature calibration of the device is presented. At the end conclusions on the calibration accuracy are outlined.

2. Device description

A photo of the chip is shown in Fig. 1 and its main properties are reported in Table 1. The chip is made of two identical cells, the reference and sample cell, respectively. Both cells consist of a 1.6 mm × 1.6 mm large and about 2 μm thick membrane. The membranes of the two cells are thermally separated by a thick Si frame of 300 μm that acts as heat sink. Two heaters are integrated in the center of the membrane. The main heater, with a resistance of about 5 kΩ, is used for the general temperature scan program. The other heater, of about 4 kΩ, is active only in power compensation mode and has to compensate for temperature differences between the reference and the sample cell. The two heaters, covered by an Aluminium (Al) layer, make up a circular area with a diameter of 0.5 mm, where the sample can be loaded. The Al layer is used to get temperature uniformity in the sample area. The temperature of the heated area is measured with an integrated thermopile. The thermal resistance (R_{th}) between the sample area and the surrounding is given by:

$$R_{th}\left[\frac{K}{W}\right] = \frac{S}{N\alpha_S} \quad (1)$$

where S is the device transfer defined as the ratio between the output voltage of the thermopile and the input power in the main heater resistance; N is the number of thermocouples forming the thermopile and α_S is the Seebeck coefficient of the thermopile. The calculated value of R_{th} is 5 kK/W at room temperature. The chip is mounted on a custom-designed ceramic base plate MultiSTAR UFS1 (24 mm × 24 mm × 0.6 mm) with 14 connections pads, and wire bonded using Al bonding wires.

Table 1
Main characteristics of Device XI400.

Symbol	Quantity	Value @ room temperature	Unit
R_{main}	Main heater resistance	5	kΩ
R_{comp}	Compensation heater resistance	4	kΩ
R_{tp}	Thermopile resistance	13	kΩ
$N\alpha_s$	Thermopile sensitivity	4	mV/K
s_a	Sample area	0.2	mm^2
L^*w	Membrane area	2.5	mm^2
τ_c	Time constant for cooling of empty sensor	12	ms
R_{amb}	Thermal resistance sample to ambient	5	kK/W
S	Transfer of chip	20.4	V/W

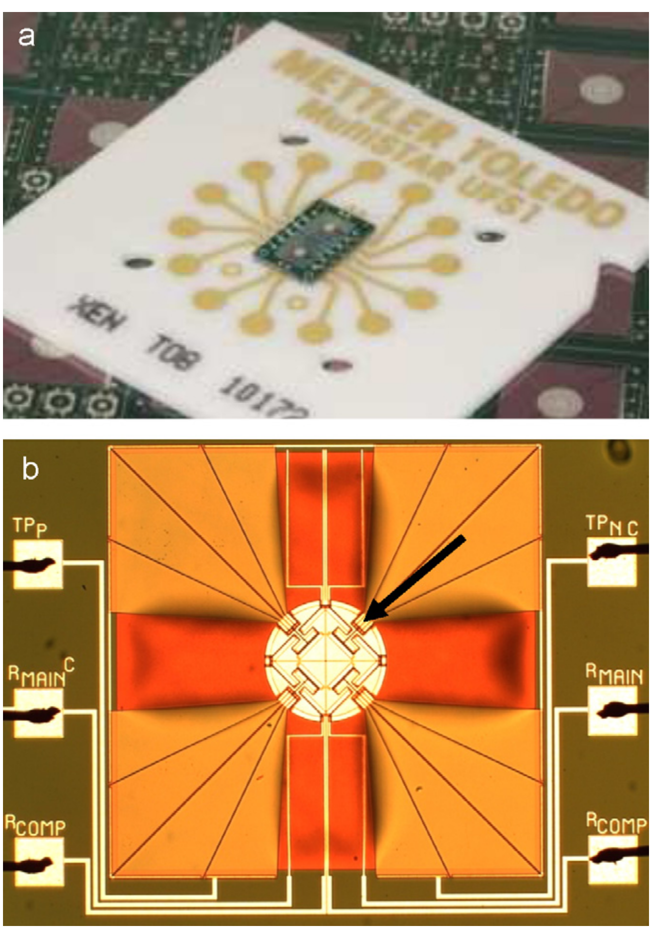

Fig. 1. Photograph of device UFS1, internal design XI400: (a) device glued on ceramic package, (b) close up of one of the two cells of the device: the heater covered with aluminium layer in the center of the membrane makes up the sample area; the hot junctions of the 8 thermocouples (2 are pointed by the arrow) are inside the sample area.

3. Electrical characterization

3.1. Main heater

The electrical resistance of the main heater (R_H) is about 5 kΩ at room temperature, with a relative standard deviation (σ) of 0.8%, calculated over 270 chips belonging to two different wafers. With a temperature coefficient of the resistance (TCR) of about 0.1%/K, the calculated σ corresponds to a deviation of about 8 K. Since the calibration method proposed in this paper is independent of the specific chip, the resistance deviation between the chips does not constitute a problem for calorimetric measurements with devices having uncalibrated heater resistance. This issue is discussed more extensively in Section 4. The time stability of the heater resistance has also been investigated. At room temperature R_H shows a variation of only 30 ppm/h. The time stability decreases with temperature, showing a drift of the main heater resistance of about 300 ppm/h at 623 K, see Fig. 2. This drift corresponds to a drift in temperature of about 0.3 K/h.

In Fig. 3 the heater resistance is shown as function of the input power. The resistance of the main heater increases with increasing heating power and thus with increasing temperature. At sample-area temperatures above 800 K the trend reverses and the resistance starts to decrease with increasing heating power. Similar behavior of the heater resistance with heating power has been found in the literature for a membrane device [13] with an n-type polysilicon heater sandwiched between a SiN and SiO_2 layer. At about 850 K the membrane cracks. The failure of the device is probably due mainly to the high stress present on the membrane caused by the different expansion coefficients of the SiN and Al layers, which are about 3.3 and 24 ppm/K, respectively. Another possible reason is the electrical breakdown of the SiN [14].