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Development of a processor embedded timing unit for the synchronized operation in KSTAR

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HIGHLIGHTS

- Timing board for the synchronized tokamak operation.
- Processor embedded distributed control system.
- Single clock source and multiple trigger signal for the plasma diagnostics.
- Delay compensation among the distributed timing boards.

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ABSTRACT

The Local Timing Unit (LTU) in KSTAR provides a single clock source and multiple trigger signals with flexible configuration. Over the past seven years, the LTU had a mechanical redesign and several firmware updates for the purpose of provision of a robust operation and precision timing signal. Now we have developed a third version of a local timing unit which has a standalone operation capability. The LTU is built in a cabinet mountable 1U PIZZA box and provides twelve signal output ports, a packet mirroring interface, and an LCD interface panel. The core functions of the LTU are implemented in a Field Programmable Gate Array (FPGA) which has an internal hardcore processor. The internal processor allows the use of Linux Operating System (OS) and the Experimental Physics and Industrial Control System (EPICS). All user level application functions are controllable through the EPICS, however the time critical internal functions are performed by the FPGA logic blocks same as the previous version. The new LTU provides pluggable output module so that we can easily extend the signal output port. The easy installation and effective replacement reduce the efforts of maintenance. This paper describes design, development, and commissioning results of the new KSTAR LTU.

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1. Introduction

The accuracy and robust operation capability of the timing system in KSTAR had been verified during for the past several campaigns. The first major upgrade of a timing system was focused on the function of FPGA [1]. Even though, we archived a high precision timing signal at the first update, the flexibility of the FPGA has allowed us to make the communication protocol more robust and increase the reliability of the entire system.

The true form-factor of the previous LTU is the PCI Mezzanine Card (PMC). It gives a good compatibility of installation for the heterogeneous control systems. We can install it on various hardware platforms like a VME, CompacPCI, PXI, and general Personal Computer by using a PMC carrier board. In recent time, however, a new concept of a time synchronization board has been required.

We occasionally find that several systems from external collaborators not following the KSTAR standard system configuration. Some nonstandard systems only available for classical coaxial cable interface. Sometimes, person in charge of the local control systems forgets the management of the LTU and did not take care of it. The resulting damage makes repairs and upgrades difficult. From a maintenance perspective, we need a more effective way to improve the ease of maintenance and deployment. Not only this reason, but we also have to secure the high density output channels for the large control system at a local site. We also considered a new function for the efficient cable interface routing.

According to the above reasons, we developed a new Local Timing Unit Version 3 (LTU3.0) as a form of 19-inch rack mountable standalone system. We decided to use a processor embedded control device for the purpose of a standalone operation capability. We

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Table 1
Specification of the new LTU3.0 next to the old.

Specification	Version 2 (2012)	Version 3
Timing resolution	Max. 5ns(1tick)	⟵
Timing jitter	<100 ps	⟵
Clock frequency	1Hz–100 MHz	⟵
Master clock	200 MHz	⟵
Outputs	8	12 (max 30)
Multi-triggering	8	50
Optical comm.	2 Gbps	⟵
Signal mirroring	No	Yes
FPGA	Spartan-6	Artix-7
IRIG-B T/C	Yes	⟵
Form-factor	PMC	Standalone
Device driver	Vxworks, Linux	Linux

have classified the hardware units by function. All components are tightly integrated to get rid of an internal cabling interface. We use a Low Voltage Differential Signaling (LVDS) cross point switch for the packet mirroring and had designed a pluggable signal output interface for easy channel expansion.

Together with the hardware itself, the control scheme has also been upgraded. Most of the local systems are automatically configured by using a timing database system. The Pulse Automation System manipulates the global shot sequence and it also controls the timing synchronization system.

In this paper, we present the results of implementation and design of the new features from the previous version of LTU.

2. Development

2.1. System features

The accuracy and resolution of the timing signal in LTU3.0 are the same as the previous version. The detailed specification is introduced on Table 1.

The LTU3.0 has twelve signal output ports in default. It is built on the two pluggable interface blades which had 6 output ports per each blade. However, the bottom side blade can be extended to 24 ports for the high density interface so that the LTU3.0 provides maximum 30 output ports.

Sometimes the gas injection system and diagnostic system require a multiple triggering functions with flexible time interval. We already implemented multi-triggering function in the previous version 2 which it supported 8 trigger signals. However, the Reflectometry diagnostic system required more flexible triggering signal, so we reconstructed the internal logic block which has a circular control scheme for the generation of a large number of triggering. The LTU3.0 currently provides a number of fifty triggers. This multi trigger function is very flexible so that we can generate triggers with equidistant or non-equidistant intervals.

A tokamak is a large scaled devices and it needs various auxiliary facilities in many places. The current timing network in KSTAR is a star topology and all LTUs were directly connected to the Central Timing Unit (CTU) through the optical switch in central control room in general. Even if two LTUs were placed in a same control room, they required two cable lines independently. Hence the additional installation of LTU was difficult. To allow for more efficient installation, we considered using of the LVDS cross point switch chip after Fiber Optic Transceiver (FOT). The LTU3.0 can deliver the timing data from the CTU to the other LTU. Fig. 1 shows current timing system interface and cable routings.

2.2. Hardware development

The key feature of Version 3 is the standalone operability. The System on a Chip (SoC) concept is widely used in a various industrial

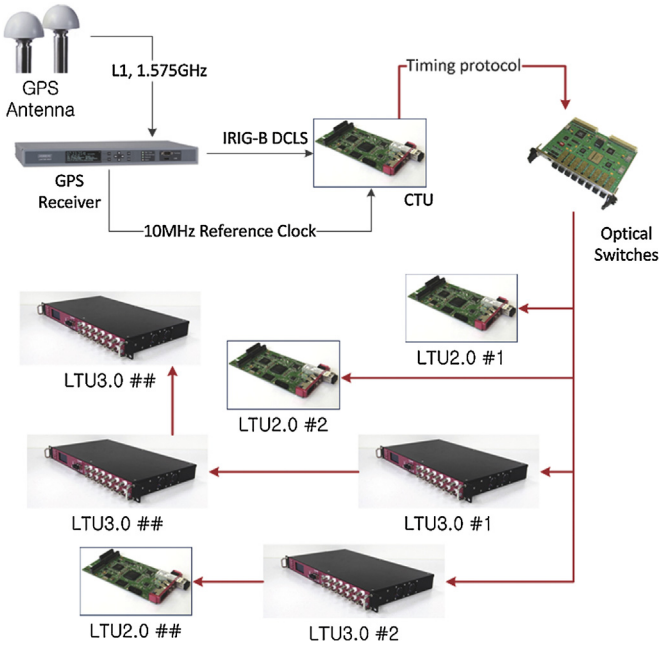

Fig. 1. Interface of timing system and cable routing.

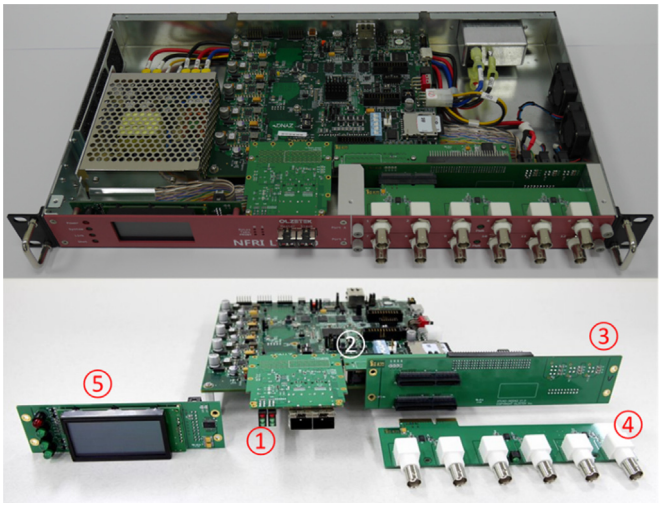

Fig. 2. Assembled component with ZC702 Evaluation Kit.

and experimental applications. Several embedded controllers are used to run diagnostics in KSTAR [2,3]. The timing delivery system in the LHD as also adopted an FPGA with a soft processor [4].

After considering the system requirement, feasibility, and cost, we chose the ZC702 from the Xilinx™. This module provides two FPGA Mezzanine Card (FMC) sites and adequate logic resources. The internal ARM® processor handles all control functions and implements a user interface in EPICS. Besides the ZC702, we developed a five of component modules.

1. Optic Communication module in FMC type
2. Bridge board between ZC702 and backplane
3. Backplane module for the signal interface
4. Pluggable output interface board
5. LCD mounted board

All customized hardware units are tightly integrated inside a homemade stainless steel case. Fig. 2 shows assembled modules in LTU3.0. The FMC standard FOT module has a single Cross Point

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