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# Fabrication, characterization and modeling of single-crystal thin film calorimeter sensors

Y. Anahory[a], M. Guihard[a], D. Smeets[a], R. Karmouch[a], F. Schiettekatte[a,*], P. Vasseur[b], P. Desjardins[b], Liang Hu[c], L.H. Allen[c], E. Leon-Gutierrez[d], J. Rodriguez-Viejo[d]

[a] Regroupement Québécois sur les Matériaux de Pointe (RQMP), Département de physique, Université de Montréal, P.O. Box 6128, Station Centre-ville, Montréal, Québec, Canada H3C 3J7

[b] Regroupement Québécois sur les Matériaux de Pointe (RQMP), Département de génie physique, École Polytechnique de Montréal, P.O. Box 6079, Station Centre-ville, Montréal, Québec, Canada H3C 3A7

[c] Coordinated Science Laboratory, Department of Materials Science and Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801, United States

[d] Grup de Nanomaterials i Microsistemes, Departament de Física, Universitat Autònoma de Barcelona, Campus UAB, 08193 Bellaterra, Spain

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ABSTRACT

Thin film based nanocalorimetry is a powerful tool to investigate nanosystems from a thermal point of view. However, nanocalorimetry is usually limited to amorphous or polycrystalline samples. Here we present a device that allows carrying out experiments on monocrystalline silicon. The monocrystalline silicon layer consists of the device layer from a silicon-on-insulator wafer and lies on a low-stress free-standing silicon nitride membrane. We applied a number of characterization techniques to determine the purity and quality of the silicon layer. All these techniques showed that the silicon surface is as pure as a standard silicon wafer and that it is susceptible to standard surface cleaning procedures. Additionally, we present a numerical model of the nanocalorimeter, which highlights that the silicon layer acts as a thermal plate thereby significantly improving thermal uniformity. This nanocalorimeter constitutes a promising device for the study of single-crystal Si surface processes and opens up an exciting new field of research in surface science.

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## 1. Introduction

By measuring the heat involved in reactions and physical transformations, calorimetry provides unique information about these processes. Many problems in nanoscience and materials engineering involving surface or near-surface phenomena can significantly benefit from this information. For example, in microelectronics, nanosized transistors depend on the interaction between silicon and a thin metallic contact [1], or on how damage induced by ion implantation interacts with dopants [2]. In chemistry, catalysis reactions occurring at surfaces are of great interest in many industrial processes. In order to study these surface phenomena, a calorimetric sensor featuring an ordered surface and sufficient sensitivity to measure reactions involving small amounts of material would be of great benefit.

Nanocalorimetry has proven most valuable in research on a wide variety of nanoscale systems during the last decade. Phenomena such as melting point depressions [3], glass transitions in polymers [4] and glass forming liquids [5], melting of self-assembled organic monolayers [6], magnetic transition in thin layers of nickel [7], and annealing of ion-implantation-induced damage [8,9] were investigated using the technique. All these experiments were carried out using devices based on free-standing low-stress silicon nitride membranes ($SiN_x$). On top of the membrane, a metal strip is patterned to heat the sample and to measure its temperature [10,11]. The sample under investigation can be deposited on the metal strip if it does not affect the electrical properties of the strip, but usually, it is deposited on the other side of the membrane, in correspondence with the heating strip. The technique has been used *in situ* with a wide variety of deposition techniques such as evaporation, sputtering, as well as ion implantation [3–9], to avoid exposure to ambient pressure and to allow carrying out measurements at low temperature and a short time after or even during deposition [3].

However, one important limitation still arises: the sample is deposited on an amorphous or polycrystalline surface, which restricts the deposited layer itself to be amorphous or polycrystalline. The observed processes may thus be significantly influenced by the microstructure of the substrate. In this article, we present a nanocalorimeter (NC) device featuring a patterned thin layer of monocrystalline silicon (c-NC). This device will allow the investigation of numerous physical processes in which the monocrystalline

* Corresponding author.
*E-mail address:* francois.schiettekatte@umontreal.ca (F. Schiettekatte).

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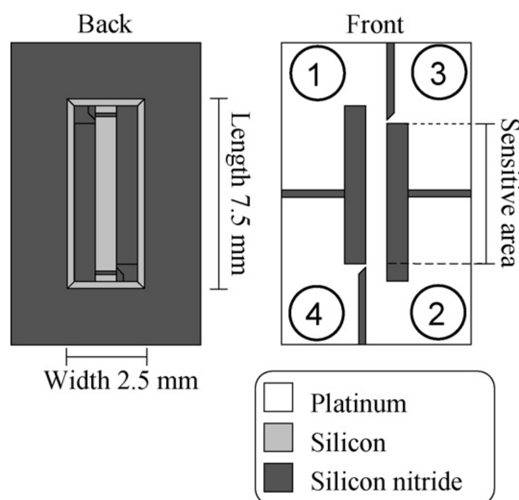


**Fig. 1.** Front and back views of the nanocalorimeter device. Current is supplied between contacts 1 and 2 while the voltage drop is measured between contacts 3 and 4.

Si surface plays a predominant role such as implantation damage annealing [8,9], 2D-to-3D strain driven transition in heteroepitaxial layers [12], agglomeration of ultra thin silicide films [13], and self-assembly of nanostructures on an ordered surface [14]. We present the c-NC fabrication technique and discuss its performances based on finite-element simulations and measurement examples. We will show that the c-Si, which offers an ordered monocrystalline and atomically flat surface, also acts as a thermal plate, therefore leading to a much more uniform temperature profile than in conventional NC devices.

## 2. Device operation

The c-NC device is compatible with conventional NC device operation explained in detail in Ref. [15]. Fig. 1 shows a schematic view of the front and back sides of the device. The sample is heated by supplying an electrical current through the platinum strip connected to pads 1 and 2. Simultaneously the voltage drop is measured by sensing point contacts that are connected to pads 3 and 4. The region of the metal strip that lies between these contacts is the part of the sensor that measures the heat capacity and will further be referred to as the *sensitive area*. The power dissipated in the sensitive area is calculated from the voltage and current measurements ($P = VI$).

The *average temperature* of the sensitive area is calculated from its resistance, $R = V/I$ which depends on temperature. The relationship between the resistance $R$ and the temperature $T$ is obtained by mounting a NC next to a thermocouple in a furnace for a calibration procedure. NC resistance and temperature are measured while the furnace temperature is changed at a rate slow enough to ensure thermal uniformity between the thermocouple and the NC. This procedure however cannot be used above $\sim$200 °C because the device supporting frame, made of c-Si, becomes conductive and alters the resistance measurement of the strip, a situation that does not happen during fast temperature scanning of the device [11]. In experiments carried out at higher temperatures, one therefore has to rely on data extrapolation for the temperature calibration. The accuracy of the calibration will be discussed in Section 5.

Prior to high temperature experiments and before temperature calibration the NCs are annealed to temperatures above the maximum experimental temperature because high temperature scans can alter the electrical properties of the heater strip. These changes influence the temperature calibration and temperature accuracy and might eventually cause device failure. One minute rapid thermal annealing of the device in inert atmosphere ($N_2$ or Ar) clearly improves device stability of the device and limits the effects mentioned above. Further stabilization can be achieved by performing a large number (500–3000) of heating cycles in high vacuum ($<10^{-6}$ Torr) prior to the experiments. A similar annealing procedure is presented in Ref. [11].

## 3. Device fabrication

Sarro et al. created a micro-device featuring a silicon island on a $SiN_x$ membrane as well [16]. Their fabrication process however requires that the silicon island is heavily n-doped and might not be suitable for silicon layer thinner than 100 nm because of etch rate uniformity. Our process yields a silicon island as pure, as smooth and as thin as the SOI device layer. The operation principle is also quite different, our design aiming at fast scanning nanocalorimetry.

A detailed description of conventional NC fabrication as well as of the calculations necessary to extract the evolution of the heat capacity of the specimen during a temperature scan can be found in Refs. [10,15]. Here, we detail the additional processing steps required for fabricating a c-NC. All steps are schematically represented in Fig. 2. The process starts with a double-side-polished silicon-on-insulator (SOI) wafer with a (1 0 0) orientation. The device layer can actually consist of any material (e.g. $Si_xGe_{1-x}$, $0 \le x \le 1$) that is compatible with the $SiN_x$ deposition process. For the devices characterized below, the handle, buried oxide, and device layers are, respectively, 300 μm, 1 μm, and 330 nm thick. A 250 nm thick layer of low-stress, high density $SiN_x$ (200 MPa tensile stress) is deposited on both sides of the SOI wafer by low-pressure chemical vapor deposition (Fig. 2a). The layer is deposited at 850 °C and 170 mTorr at a rate of 3 nm/min using $SiCl_2H_2$ and $NH_3$ gases at a flow of 57 and 13 sccm, respectively.

The subsequent steps consist in depositing and patterning the metal strip (here made of Pt). These steps are similar to those described by Karmouch et al. [10], except that the Ti adhesion layer is replaced by Cr because of its resistance against subsequent hydrofluoric acid (HF) etching steps (Fig. 2b).

A cavity is then etched from the backside of the NC (Fig. 2c). A photoresist mask is patterned, aligned with the metal pattern on the front side. The $SiN_x$ layer is removed by reactive ion etching (RIE) using $SF_6$ and He flowing at 26 and 14 sccm, respectively, and setting the power of the plasma to 250 W. The oxide is removed in HF and a cavity in the Si handle is anisotropically wet etched using a tetramethylammonium hydroxide (TMAH) solution. This etch will stop on the buried oxide. The exposed oxide layer is subsequently removed using HF etching (Fig. 2d).

The last step in the fabrication process consists in patterning the silicon strip. Photoresist (Shipley S1813) is carefully deposited at the bottom of the cavity, spin-coated at 3000 rpm for 30 s and soft-baked at 115 °C for 90 s. Exposure to UV light is carried out using a shadow mask. While exposure might be blurred due to the distance between the shadow mask and the bottom of the cavity, the photoresist offers sufficient contrast to result in a well-defined pattern. The photoresist is developed in a liquid solution (Shipley MF-319) for 90 s (Fig. 2e). Silicon is then etched by RIE using $SF_6$ flowing at 26 sccm at a power of 100 W for 14 min. In these conditions, silicon is etched at a rate at least five times higher than $SiN_x$ thus providing sufficient selectivity to etch entirely the silicon layer without damaging the membrane. The remaining photoresist is first dissolved in acetone, then in N-methyl pyrolidinone for 5 min and is finally completely removed in an $O_2$ plasma at 300 W for 20 min (Fig. 2f). Extra HF etching can be carried out just before

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