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Analysis of fault current contribution of Doubly-Fed Induction Generator Wind Turbines during unbalanced grid faults

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ABSTRACT

The fault current contribution of the Doubly-Fed Induction Generator Wind Turbines (DFIG-WTs) under unbalanced grid faults did not draw researchers' attention due to the absence of any related requirements in the former grid codes. However, in 2015 new requirements were established dictating the DFIG-WT/generating unit to remain connected to the grid during phase-to-phase short-circuit and to perform reactive power provision. Thereupon, the knowledge of the fault current magnitude as well as the dynamic response of the DFIG-WT are crucial for the power system component design and for the validation of its commitment to the grid codes requirements. There are concrete control objectives regarding negative sequence control that cannot be fulfilled simultaneously but rather set according to the owner's preferences. Therefore, in this paper, a detailed analysis of the negative sequence current response under each control objective were carried out, considering all the controller parameters. The influence of each controller structure on the short-circuit quantities is investigated and based on it an approximated mathematical models of the short-circuit quantities and currents were proposed. Finally, a brief analysis, due to space limitation, of the response during the voltage limitation period is also performed where the influences of voltage limitation on the negative sequence current were shown.

1. Introduction

Wind power has established itself as a main source for the generation of electricity in the past decade by delivering at least 3.4% of the world's electricity in 2014, a figure expected to increase to 6–8% by 2020 and to 8–17% by 2030 [1,2]. There are five different Wind Turbine (WT) technologies available on the market, whereas DFIG-WT represents the highest proportion of WT installations worldwide [3]. The DFIG-WT has major features such as a partial-rated converter which allows a variable speed operation over a typical range of ±30% of the synchronous speed, decoupled control of active and reactive power and voltage support capabilities.

A typical layout of a DFIG-WT is illustrated in Fig. 1. The stator is directly connected to the grid via a step-up transformer of two or three windings -depending on the machine's rating-, whereas the rotor is connected to a back-to-back voltage source converter (VSC). The machine side converter (MSC) supplies the rotor with 3-phase voltages of variable magnitude, frequency and phase angle. Thus, along with the pitch control of the rotor blades, it enables variable speed operation for maximum energy utilization and fast control of active and reactive power. On the other side, the line side converter (LSC) allows for bi-directional power flow by maintaining the DC link voltage at a predefined constant value, and also allows for grid voltage support during disturbance periods.

For economic competence, the VSC is designed with limited voltage and thermal capability. In order to comply with the grid code requirements during Fault Ride-Through (FRT) [4], a low cost and effective protection scheme is implemented. This protection scheme incorporates a chopper circuit connected to the DC link to protect the IGBTs against high DC voltages and excessive currents in the rotor circuit [5]. Additionally, it incorporates a crowbar circuit connected to the rotor for protection against excessive currents. However, the crowbar operation is not desired due to the long deactivation period of the MSC accompanied with it, which leads to loss of controllability.

An optimum setting of the protective devices as well as optimal design of the power system components (circuit breakers, bus-bars, etc.) require the knowledge of the fault current magnitude, which is expected to reach a maximum peak value during 3-phase short-circuit. However, for the DFIG-WT without dedicated negative

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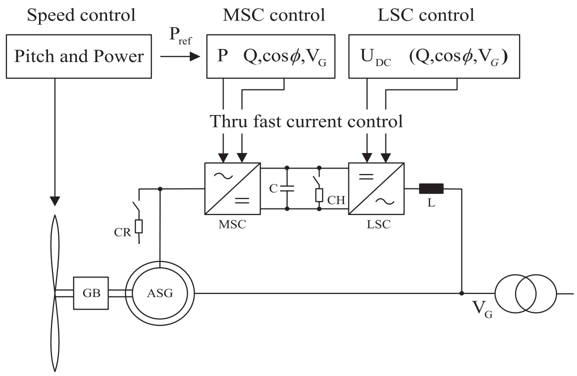

Fig. 1. DFIG-WT system configuration.

sequence control, the maximum peak of the fault current occurs during unbalanced faults. This is attributed to the low negative sequence transient impedance of the DFIG. The behavior of the DFIG-WT during balanced fault has been reported in many publications [6–8]. However, no attention was paid to the behavior during unbalanced faults, because the former grid codes were not indistinct [9] or did not even have specific requirements [10] regarding negative sequence currents supplied by the WT, even though the occurrence of unbalanced faults reaches up to 90% of fault types [11]. In 2015 the VDE has established new requirements regarding connection of private generation facilities connected to the public high-voltage network [12].The new requirements set new criterions regarding FRT during 2-phase short-circuit. According to the new requirements the generating units must remain connected in the entire operating range as long as the phase-to-phase voltages at the grid connection point within the boundaries of the curve shown in Fig. 2. Additionally, the generating units must support the grid voltage through reactive current provision, which magnitude is proportional to the voltage deviation as shown in Fig. 3.

The occurrence of unbalanced voltage at the DFIG-WT terminals produces additional torque that increases the value of the load torque and leads to an increase in core losses. The negative sequence currents result in non-uniform distribution of the power losses, which leads to local winding overheating and consequently decreases the machine life expectancy [13]. Additionally, the interaction between the sequence components creates pulsating torque on the shaft, causing audible noises and extra mechanical stress [14].

Several control methods have been proposed to solve the aforementioned problems. Some of these methods use a resonant/low-pass filter or signal delay cancelation in combination with a PI-controller to extract and compensate the negative sequence

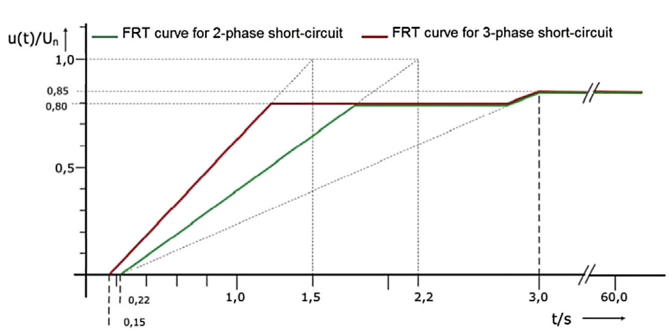

Fig. 2. New FRT requirements according to VDE.

components [15], while others use a proportional integral-resonant (PI-R) controller for direct compensation [16]. However, the first methods have poor dynamics while the second does not allow for the possibility to set a priority for the controller. The limitations and capabilities of negative sequence control are investigated in Refs. [17–19], where it was shown that the available control for negative sequence voltage reaches its limits close to the upper and lower speed ranges. In addition, the negative sequence current reduction allows higher positive sequence currents. The analysis of the DFIG-WT behavior under unbalanced faults has been carried out in Refs. [20,21] but without any mathematical/analytical justification for the results. The only mathematical interpretation was provided in Ref. [22] but the analyses were unsubstantiated, neither by experiment nor by simulation.

There are concrete control objectives regarding negative sequence control that can be fulfilled one at a time [14]. For the MSC, these are:

a) No negative sequence compensation
b) Compensation of negative sequence currents
c) Compensation of pulsating torque

and for the LSC:

d) Compensation of negative sequence current
e) Compensation of DC circuit voltage pulsation

None of these control objectives stands out from the others. This is related to several facts for instance, if a full compensation of negative sequence currents is achieved there will be no residual currents left to sense by protection devices [23]. For the MSC the compensation of the pulsating torque requires prioritization of the negative sequence controller. In that case, the voltage reduction in the positive sequence would lead to conflict with the grid code requirements. For the LSC it is advantageous to operate the LSC with balanced current to avoid non-uniform power losses. However, high voltage pulsation decreases the service life of the capacitor [14].

The new FRT requirements regarding behavior during unbalanced faults [12] require the knowledge of the DFIG-WT response, in order to verify the compliance to the requirements. Therefore, in this paper a detailed analysis of DFIG-WT response during unbalanced faults supported by simulation results is performed for each control objective considering the controller's influences on short-circuit parameters. The analysis introduced in this paper is a continuation of previous work reported in Refs. [24–26] regarding the DFIG-WT fault response. The inadequacy of the IEC-60909 or current methods proposed for estimating the fault current contribution was provided in Refs. [24,25], while in Ref. [26] a detailed analysis of the response during balanced fault were carried out. Based on the analysis a new mathematical model describing the fault behavior is provided. Consequently, based on the analysis carried out in this work, an expression describing the negative sequence fault current of the DFIG-WT is developed.

2. Simulation network

Fig. 4 shows the simulation network used in this paper, where a manufacturer based simulation model of DFIG-WT (real–world parameters are used, so that the results reflect the real dynamic behavior as closely as possible) is implemented. A phase-to-phase fault is applied at the middle section of the cable, which results in negative sequence voltage at the PCC of 0.2 p.u magnitude. Prior to the fault, the DFIG-WT was operating in super-synchronous mode with 0.6 p.u active power, −0.1 slip and unity power factor.