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Minority carrier lifetime and efficiency improvement of multicrystalline silicon solar cells by two-step process

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ABSTRACT

Impurities and defects are of significant interest in multicrystalline silicon, due to the detrimental effect they can have on carrier lifetimes and electrical properties. In view of that, it is important to incorporate certain processing steps to decrease the recombination activities. In this study, a novel experiment was applied as a beneficial approach to improve the electronic quality of low-resistivity mc-Si substrates via a two-step process. Initially, the first step involves gettering multicrystalline substrates using sacrificial porous silicon layer on both sides, which was introduced as a simple sequence for efficient extrinsic gettering schemes. The gettering experiment was performed at 600–900 °C, and optimum results were obtained at 900 °C. Then, the second step involves coating the front surface of gettered mc-Si at 900 °C with vanadium oxide that serves as an excellent antireflection layer and leads to improve furthermore the electrical properties. Significant improvements were obtained after the deposition of vanadium oxide antireflection coating, in view of the fact that gettered mc-Si substrate at 900 °C provides the highest minority carrier lifetime and the lowest effective surface recombination velocity. An overall increase of the electrical properties was obtained after the described two-step process. The conversion efficiency increases from 6% (reference) and reached 13.7%.

1. Introduction

Multicrystalline silicon solar cells performance is mainly limited by minority carrier recombination at dislocations and intragrain defects such as certain impurities or precipitates. These impurities can be contained in the silicon feedstock used to grow multicrystalline silicon (mc-Si) ingots, since it comes chiefly from silicon rejects from the microelectronics industry. The presence of electric active grain boundaries in multicrystalline silicon is a serious limitation for the photovoltaic (PV) efficiency. Due to the high densities of defects and metallic impurities, additional steps are needed to improve the quality of mc-Si substrates [1]. The possibility of improving the electrical properties of silicon wafers, by extracting impurities from them, using thermal treatment under oxygen atmosphere, or phosphorus diffusion, is well known. Besides, the porous silicon (PS) layer may be used as an efficient sacrificial layer for gettering metallic impurities [2–5]. High-temperature annealing of the chemically etched porous silicon enhances the impurity diffusion into the porous silicon network, thereby acting as an efficient external gettering site and impurities can be accommodated inside the cavities of the porous silicon network. The efficiency of a solar cell is mainly related to the reflectivity of the wafer surface, absorption of incident photons and their conversion into electrical current. A good anti-reflective coating (ARC) is vital for solar cell performance as it ensures a high photocurrent by minimising reflectance [6,7].

To increase the conversion efficiency, antireflection coating, light trapping and surface passivations must be taken into account. Vanadium oxide has been used as an antireflection coating and to passivate the front surface of mc-Si solar cells, grain boundaries (GBs) and porous silicon [8,9] and make the possibility of combining in one processing step an antireflection coating deposition along with efficient surface state passivation, as compared to a reference wafer. The aim of this work is to investigate the effect of two-step treatments, gettering mc-Si substrates prior to the deposition of vanadium oxide antireflection layer at the front surface, what led to an important improvement of the electrical properties and consequently the conversion efficiency.

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2. Experimental details

The experiments were carried out on p-type boron doped multicrystalline silicon substrates with a bulk resistivity of 0.5–2.0 Ω cm and a thickness of about 400-μm. The surface area of used substrates is 3.6 cm^2. Samples were selected from consecutive mc-Si wafers sharpened successively in the same ingot Therefore, differences between sister wafers after different processing can be interpreted as being due to variations in the process parameters, rather than due to material variations. In order to obtain a cleaned surface, required for homogeneous porous layer formation, Wafers were dipped for a few seconds in an acid mixture solution (HF: 16%, HNO_3: 64%, CH_3COOH: 20%).

Multicrystalline silicon (mc-Si) samples have been divided into two sets, as described in Fig. 1. PS layers were formed on both sides by the stain-etching technique using $HF/HNO_3/H_2O$ solution with a 1:3:5 volume composition. The PS formation is then followed by a photo-thermal heating process. The samples are placed in a closed quartz reactor, then, introduced into an infrared tubular furnace equipped with infrared lamps. Thermal annealing was performed at different temperatures, during 60 min under an O_2 atmosphere. The aim of this thermal treatment was to concentrate the unwanted impurities in the inactive region (the formed porous silicon layer on both sides of the substrates). In order to eliminate the forming silicon oxide layer and to remove the PS structure, after annealing, we immerse these samples successively in an HF and a NaOH (1N) solution. Thermal treatments are all ranging between 600 °C and 900 °C for 30 min. Thereafter, deposited antireflection layer was achieved using vanadium pentoxide (V_2O_5) powder, which was thermally evaporated under vacuum (at 10^{-5} Torr) by Joule effect. The Powder to be evaporated was put on conductive (tungsten) crucible and the distance crucible-sample was adjusted at 20 cm. Coated mc-Si substrates with vanadium oxide antireflection layer were subjected to a thermal treatment to activate furthermore the passivation process (Fig. 1).

The effect of the gettering procedure was investigated by means of the effective minority carrier lifetime (τ_{eff}), measured using WTC120 lifetime tester. The chemical composition of the deposited vanadium oxide thin films was analyzed by means of Fourier Transform Infrared Spectroscopy (FTIR). Surface and cross-section morphology were determined by a scanning electron microscope (SEM). To achieve the mc-Si solar cells, n-type front emitter junction was achieved by the use of $POCl_3$ diffusion in a rapid thermal infrared tubular furnace. The back aluminum (Ag/Al) and the front Ag contact were screen printed and fired at 850 °C and 620 °C, respectively.

3. Results and discussion

The minority carrier lifetime is considered as an important parameter that defines the quality of the crystalline silicon substrates. The measured τ_{eff} takes into account the recombination

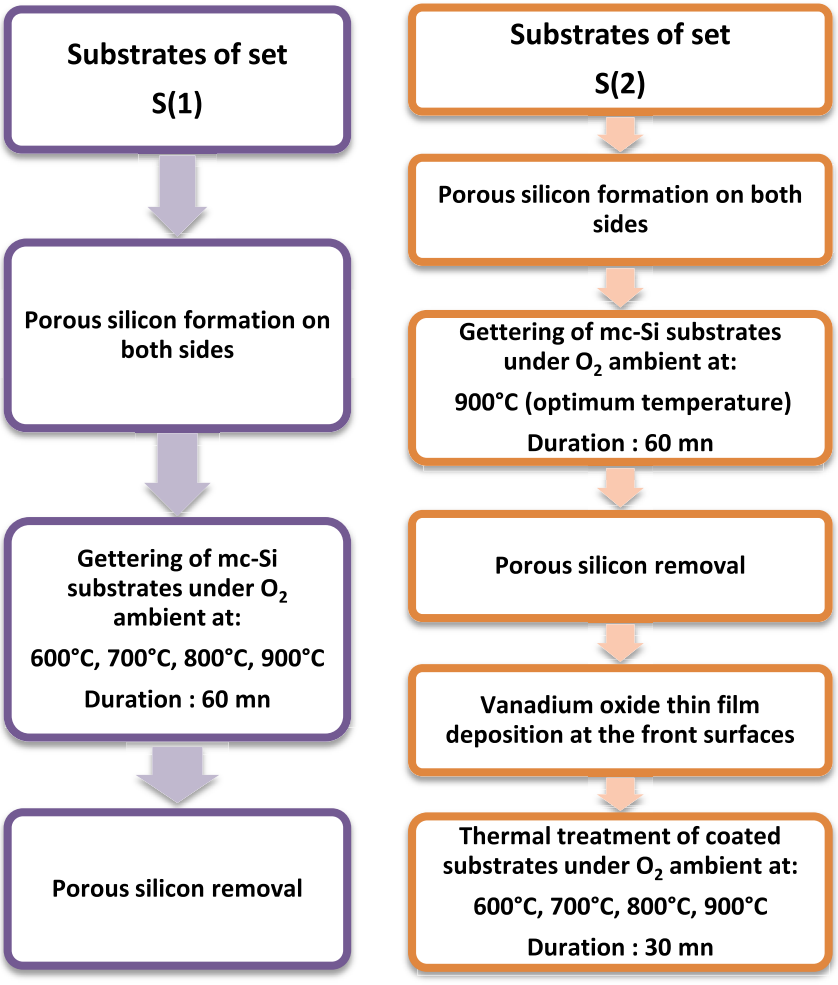

Fig. 1. Applied process sequences in sets (S1) and (S2).