Renewable Energy 78 (2015) 590–598

Contents lists available at ScienceDirect

Renewable Energy

journal homepage: www.elsevier.com/locate/renene

The effect of front pyramid heights on the efficiency of homogeneously textured inline-diffused screen-printed monocrystalline silicon wafer solar cells

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ARTICLE INFO

Article history:
Received 31 March 2014
Accepted 23 January 2015
Available online

Keywords:
Monocrystalline silicon wafer solar cells
Homogeneous texturing
Different pyramid heights
Potassium silicate
Inline-diffused screen-printed cells
Contact resistance

ABSTRACT

The majority of industrial monocrystalline silicon (c-Si) wafer solar cells are alkaline textured (at least the illuminated surface) to reduce reflection and increase absorption of incident light. Therefore, understanding the influence of front pyramid heights on the solar cell parameters is essential for further improving cell efficiency. In this work we report the impact of pyramid height on the performance of inline-diffused c-Si solar cells. Three alkaline texture processes with potassium silicate additives are optimised to result in homogeneous coverage of pyramids. By modifying the process, surface textures with small (~5 μm maximum), medium (~6 μm maximum) and large (~8 μm maximum) pyramid heights are formed. The impact of pyramid size on cell parameters is experimentally studied using industrial-grade 156-mm pseudo-square *p*-type Czochralski wafers. It is found that within the pyramid size range studied here, there is no significant variation in effective minority carrier lifetime, reflectance, open-circuit voltage or short-circuit current. However, fill factor and hence efficiency is significantly impacted by pyramid size. While cells in all three groups demonstrate high fill factor (>79%), it is shown that an average fill factor gain of up to 1% absolute can be achieved by using the best-suited texture process.

1. Introduction

The large availability of crystalline silicon (both mono and multi) wafers helps in rapid expansion of the global photovoltaic market. The key challenge for monocrystalline silicon (mono-Si) wafer solar cell is further reduction of the dollar per Watt cost. A route to achieve higher solar cell efficiency is optimisation of key processes, such as an alkaline texturisation. The textured surface, due to the so-called 'double-bounce' effect, reduces the reflectance from the illuminated surface [1–3]. The anisotropic selective chemical etching of the <100> Si surface with sodium hydroxide (NaOH) or potassium hydroxide (KOH) solutions has been used to form random upright pyramidal textured surface [1]. Iso-propyl alcohol (IPA) is commonly added to the alkaline texture solution; it modifies the surface wettability to controllably nucleate the texturing process [4] and thus helped to achieve good lateral uniformity of the pyramids across the entire wafer. Recently Basu et al. [5] have used potassium silicate (K_2SiO_3) as an additive to the alkaline textured solution. This advanced solution reduces IPA consumption, while enhancing texturing process; thus, increases throughput.

Previous studies have analysed the influence of pyramid height on the solar cell performance by simulations or experiments [6–11]. From a geometric optics (ray tracing) point-of-view the size of regular upright pyramids does not affect the front surface reflectance and the obtained short circuit current (J_{sc}). However the geometric optics simulation approach is only valid when surface feature sizes are larger than the interacting wavelength, this condition is not strictly fulfilled for solar cells as wavelengths up to 1100 nm are relevant for crystalline silicon solar cells and random pyramid texture processes may lead to some sub-micrometre pyramids. A rigorous simulation study by Llopis and Tobías [6]

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http://dx.doi.org/10.1016/j.renene.2015.01.058
0960-1481/

involving numerical solution of the electromagnetic wave equations concluded that diffraction effects are significant only for pyramid smaller than 300 nm, in this case the reflectance increases beyond the geometric optic limit. Typically simulation studies are limited to include the effects of the pyramids size distribution and therefore experimental studies provide better insights on this effect on the solar cell's optical performance. In terms of open-circuit voltage (V_{oc}) pyramidal textured surfaces increase surface recombination due to an enhancement of surface area (corresponding to the planar surface). For pyramids of standard geometry the area enhancement is independent of the pyramid size (if the surfaces are fully textured) and no effect on V_{oc} is expected. The influence of pyramid sizes on the fill factor (*FF*) has been studied, however contradicted results were reported. Cabrera et al. [7] and Han et al. [8] observed reduction in *FF* for pyramid sizes smaller than 300 nm. However, while Cabrera et al. observed no impact of pyramid height (KOH–IPA texture chemistry) on *FF* for pyramids larger than 300 nm [7]. Han et al. [8] observed a variation in *FF* without a clear trend (NaOH–IPA + variable additives). Note that modification of the pyramids size can resulted with non-uniformity of the texturing. Ximello et al. [9] used an alkaline texture process based on a KOH and "high boiling alcohol (HBA)" process chemistry (different from standard KOH–IPA chemistry) and varied texture time to generate different pyramid sizes. Although a significant variation was observed in J_{sc}, V_{oc} and *FF* [9], the variations were attributed to texture uniformity.

Other studies focused only on the impact of the pyramid size. For examples, King and Buck [10] investigated only the impact on front surface reflectance, while Kegel et al. [11] studied the influence on intrinsic amorphous-Si passivation for heterojunction cells. It seems that comprehensive study regarding the impact of pyramids height on the solar cell electrical parameters is required.

In this study, three different texturing recipes were developed to generate three different homogeneous pyramidal structures with maximum heights varying from 5 μm to 8 μm, with good uniformity of pyramid heights within each group. The pyramids size was controlled by varying the alkali concentration, the texturing temperature and the amount of potassium silicate in the KOH–IPA solution. It was found that textured wafers from all the three groups have similar solar spectrum weighted average reflectance (WAR) in the range of 11.5–11.8%. Wafers from all groups were used to fabricate conventional 156 mm pseudo-square inline-diffused screen-printed solar cell with average efficiencies in the range 18.4–18.6%, using the pilot line at the Solar Energy Research Institute of Singapore (SERIS). Details and characterisation of the new texturing process and the resulting solar cells will be presented, including scanning electron microscope (SEM) images, reflectance, quasi-steady state photoconductance (QSSPC) and contact resistance measurements, series resistance imaging from a combination of photoluminescence (PL) and electroluminescence (EL) images, and 1-Sun *I*–*V* measurements.

2. Experimental details

2.1. Texturisation

In this experiment 150 wafers of industrial grade monocrystalline Cz silicon wafers were used (156 mm pseudo-square, *p*-type, boron doped, <100> orientation, 1-2 Ω-cm resistivity, 170–190 μm thickness). Pre-cleaning and damage removal process of the wafers prior the texturing was performed following the process developed by Basu et al. [12]. It used KOH (20% by weight) and sodium hypochlorite (NaOCl) solution in a ratio of 1:3 (by volume). The wafers were immersed in the solution for 2 min (min) at 80 °C to remove the surface damage (~3 μm per side, as measured by measuring the change of the wafer's weight). The wafers were split into three groups of 50 wafers each, corresponding to three different pyramid heights (groups A, B and C). A mixture of KOH, IPA and K_2SiO_3 was used to form homogeneous (or uniform) pyramidally textured surfaces [5]. The texturing chemical bath was made from polyvinylidene difluoride (PVDF) material and was heated from the bottom by a flat Teflon coated heater. This bath is an overflow bath fitted with an external pump which circulates the texturing solution in order to minimise variation of the solution concentration and temperature. The texturing solution temperatures were maintained at a constant value of 80 °C and 85 °C corresponding to different texturisation recipes. However, the texturing time maintained constant as 20 min for all the processes. In this study, the KOH concentration was varied from 1.4% to 2.5% (by weight), while the amount of K_2SiO_3 and IPA were varied from 60 to 100 ml and from 2.5 to 3.2 L, respectively in a 40 L bath.

After texturing, all the wafers were neutralised in 1:1 solution of hydrochloric (HCl) acid and de-ionised (DI) water at 60 °C for 10 min followed by a dip in dilute hydrofluoric acid (HF). The complete process flow of the different groups is shown in Fig. 1. Following the texturing, the wafers were processed together as a single batch.

2.2. Cell fabrication

The textured wafers were diffused in an industrial inline-diffusion furnace (Despatch, DCF-3615). After an atmospheric-plasma pre-treatment step at the entry to the doper (to create a hydrophilic Si surface), a spray-on dopant source was applied uniformly to both sides of the wafer at 30 L/min rate [ortho-phosphoric acid (H_3PO_4) mixed with ethyl alcohol]. The diffusion was performed at a belt speed of 390 mm/min using a peak diffusion temperature of 895 °C for all the wafers to achieve an emitter sheet resistance (R_{sq}) of ~40 Ω/sq, as measured by four-point-probe measurements (Cresbox, NAPSON). The parasitic rear-junction and the front phosphosilicate glass (PSG) were removed in an industrial inline wet chemical tool (InPilot, RENA GmbH) using solution mixture of HF, nitric acid (HNO_3) and sulphuric acid (H_2SO_4) at 6–8 °C. The etch-back was performed using 'SERIS etch' [13,14] to achieve the targeted final R_{sq} of ~70 Ω/sq. Amorphous silicon nitride (SiN_x) antireflection coating (ARC) was then deposited onto the front surface using an industrial plasma enhanced chemical vapour deposition (PECVD) system from Roth & Rau (SiNA-XS). The film thickness and refractive index (at 633 nm) were measured to be 70 nm and 2.05, respectively. Lastly, front and rear contacts were formed by screen printing (PVP1200, DEK) and subsequently co-fired in an industrial fast firing furnace (Ultraflex, Despatch), using a Monocrystal PASE 12D aluminium (Al) paste for the rear and DuPont PV17F Ag paste for the front contacts. The summary of the complete cell fabrication process flow is shown in Fig. 2.

2.3. Characterisation

Representative samples from the three groups were removed after various process stages for additional surface characterisation studies. Prior to these measurements, the representative samples were cleaned in IPA, followed by DI rinsing and drying. A scanning electron microscope (SEM) from Carl Zeiss Auriga was used for the surface topography analysis and a spectrophotometer (Perkin Elmer, Lambda 950) was used for the reflectance measurement. For calculation of the WAR, the diffuse reflectance of the textured surfaces was measured using a 150 mm diameter integrating sphere over the wavelength range of 300–1000 nm and weighted with the AM1.5 spectrum. The effective minority carrier lifetime was subsequently measured using a lifetime tester (Sinton