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An optimized reconfigurable algorithm for FPGA architecture oriented IoT applications

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Abstract

Application Specific Integrated Circuit (ASIC) can facilitate the user with high speed, but a small modification in the algorithm and architecture will lead to more cost in terms of design and development. In contrast Field Programmable Gate Array (FPGA) provides near optimal speed with reconfigurability of algorithm/architecture at any time. From research survey, we come to conclusion that Fast Fourier Transform (FFT) plays critical role in many applications such as Orthogonal Frequency Division Multiplexing (OFDM), image processing application and signal processing application. In this paper, we have developed a reconfigurable FPGA architecture for FFT algorithm. Also, reconfigurable algorithm is proposed to handover the reconfiguration control, so that the datapath can be changed. The proposed reconfigurable FPGA architecture is developed using Verilog and targeted in Altera FPGA boards. The evaluation and comparison of the proposed architecture shows remarkable improvement in terms of throughput, area and power.
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Keywords: ASIC; Reconfigurable FPGA; FFT; Throughput

1. Introduction

The available cost and speed in demand have a great impact on solving many practical problems. Application Specific Integrated Circuit (ASIC) plays hands on role in developing high speed application, if and only the algorithm is fixed. The speed of ASIC is not comparable, until the algorithm is changed. And there is a need of expensive/complicated modification, if the algorithm/architecture is changed. A general purpose processor is more successful, if the application speed is not a constraint. The change in algorithm/architecture can be easily handled, since the general purpose processor is more flexible than ASIC. Another vital factor to consider is that the area, if the available area is high then the overhead due to pipeline/parallel processing is easy. On the other hand, the ASIC has lesser area, since it is application specific and cannot handle the task overhead.

Here comes the FPGA (Field Programmable Gate Array), that can allow more flexibility and adaptability to the user. We can develop the any application specific process in the FPGA platform and the algorithm/architecture can be modified during runtime or permanently. In FPGA, there is no problem with area, since we can choose the FPGA device according to the application and the speed is near optimal to ASIC. In order to develop reconfigurable architecture, the application must be fixed. In Tang, Liao, and Chang (2012), the Fast Fourier Transform (FFT) for Wireless Personal Area Network (WPAN) application is developed. The designed FFT consumes 507 mW running at 300 MHz frequency with the speed of 2.4GS/s. In

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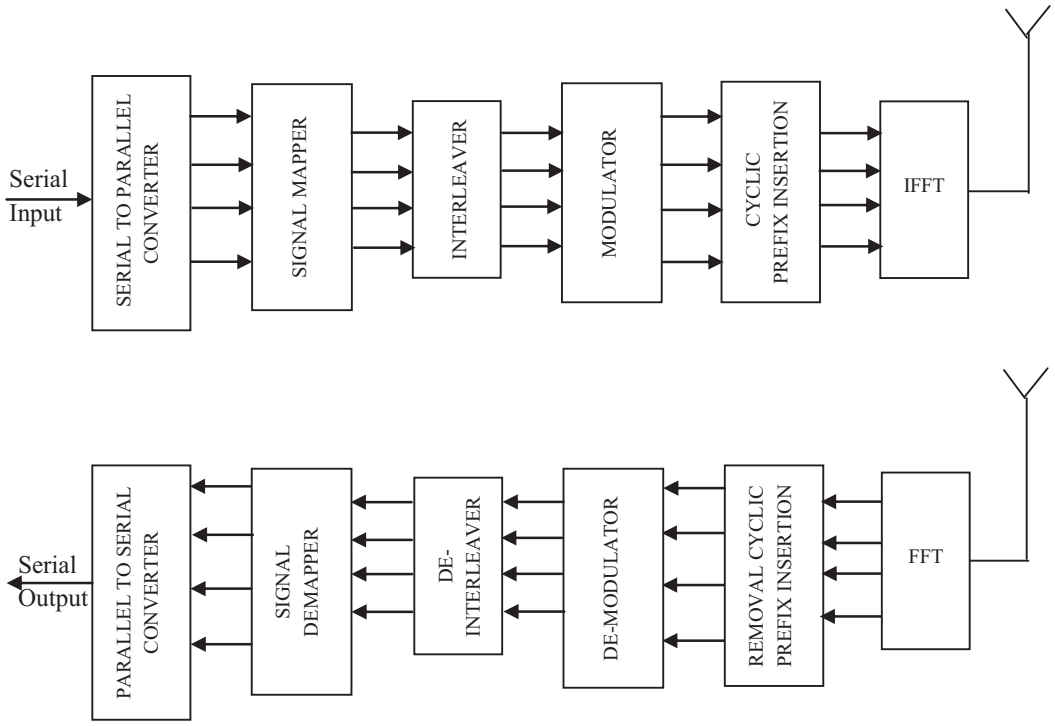

Fig. 1. OFDM application.

Guan, Fei, and Lin (2012), the FFT is designed for Orthogonal Frequency Division Multiplexing (OFDM) that consumes a power of 60.7 mW and area of 147k gate element. The FFT computation of real signal is performed by developing parallel/pipelined architecture (Salehi, Amirfattahi, & Parhi, 2013), considering the real data path is one of the key role in this architecture. However, this methodology consumes high power, delay and logic elements. The idea of using GPU (Graphical Processing Unit) to compute the FFT is limited by its data transfer rate and memory size. In Chen and Li (2013), hybrid parallel framework has been introduced to overcome this problem and remarkable speed is achieved. The need of Digital Audio Broadcast (DAB) receiver has been fulfilled by CSPD (Circuit Sharing Pipelined design) (Wang and Lin, 2007), which are more efficient than its previous version of Circuit Sharing Design (CSD). This design possesses lesser gate count, reduces redundancies in circuit and occupies small memory size. The FFT has another problem of more store and load operations, this limitation is overcome by developing extended split-radix FFT (Takahashi, 2001). The extended split-radix FFT is more efficient in terms of computational complexity, load and store operation when compared to conventional FFT algorithm.

The computation efficient pruning FFT is proposed in Wang, Zhou, Sobelman, & Liu (2012), according to pruning logic, there is no need of computation for input values that are zero and also the output values in some regards are not involved for further computations. The process of pre-multiplication and successive decomposition is used to develop array architecture (You and Wong, 1993) that will compute the FFT very fast. The radix 2^5 FFT processor is proposed in Cho and Lee (2013a), the processor runs at the frequency of 310 MHz with the throughput rate of 2.5GS/s consuming 290k gate count. High speed and low are FFT architecture is proposed in Jiang, Luo, Tian, & Song (2005) for OFDM, in addition, dual and parallel butterfly algorithm is utilized in the architecture. The achieved results confirm that the proposed FFT can be utilized in IEEE 802.11a standard. The radix-2, 4 FFT computations is reduced by utilizing multi-path delay commutators (Cheng and Parhi, 2007), which require lesser logical elements. The FFT for OFDM is developed by pipelined approach that achieves a high throughput rate. The proposed FFT (Tang, Tsai, & Chang, 2010) runs at the frequency of 300 MHz, with the speed of 2.4GS/s consumes a power of 159 mW. Although many work have been contributed in FFT in terms of speed, throughput, computation, area, there is minimal research have been done in reconfigurable FFT. In this work, we are going to develop a reconfigurable FPGA architecture for Fast Fourier Transform (FFT). The simple application of FFT in Orthogonal Frequency Division Multiplexing (OFDM) is shown in Fig. 1.

2. Problem identification

In general, the 64-point FFT is processed with butterfly unit, where the twiddle factor for butterfly computation is stored in the Read Only Memory (ROM). The intermediate results from R_1 are stored in the register r0 to r15. Then, it is used for the next stage, which is R_2 for further processing as shown in Fig. 2. The major drawback in the

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