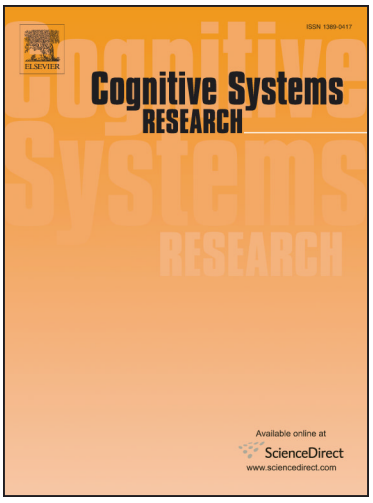

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PII: S1389-0417(17)30118-3
DOI: https://doi.org/10.1016/j.cogsys.2017.12.001
Reference: COGSYS 592

To appear in: *Cognitive Systems Research*

Received Date: 15 April 2017
Revised Date: 31 August 2017
Accepted Date: 1 December 2017

Please cite this article as: Xu, J., Liu, Z., Jiang, J., Dou, Y., High Performance Robust Audio Event Recognition System Based on FPGA Platform, *Cognitive Systems Research* (2017), doi: https://doi.org/10.1016/j.cogsys.2017.12.001

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Abstract

Audio event recognition is applied in many novel application areas. Opposing the deep CNN, 1-max pooling CNN is a simple, but efficient CNN architecture for robust audio event recognition. This study proposes a parallel architecture to accelerate robust audio event recognition. To implement this in hardware, we evaluate the precision of 1-max pooling CNN model and propose an approximate algorithm to replace the complex calculation in spectral image feature (SIF) extraction. We then propose a scalable parallel structure of SIF extraction and 1-max pooling CNN. The SIF extraction unit has eight parallelisms and the 1-Max Pooling CNN accelerator has 40 processor elements (PEs) in our implementation. The entire system is implemented on the Xilinx VC709 board. The average performance of our FPGA accelerator is 675.7 fps under 100 MHz working frequency, which is about 31.9× speed-up compare with CPU. We further implement a small-scale FPGA array with four Xilinx FPGA for robust audio event recognition. To communicate between the four FPGA and the host, we design a route protocol based on source route algorithm.

Keywords: Audio event recognition, convolutional neural networks, 1-max pooling, precision evaluation, parallel architecture, FPGA

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