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Output feedback control of asynchronous sequential machines with disturbance inputs

Jung-Min Yang [a], Seong Woo Kwak [b,*]

[a] School of Electronics Engineering, Kyungpook National University, 1370 Sankyuk-dong, Buk-gu, Daegu 702-701, Republic of Korea
[b] Department of Electronic Engineering, Keimyung University, Sin-Dang-Dong 1000, Dal-Seo-Gu, Daegu 704-701, Republic of Korea

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ABSTRACT

This paper presents a control scheme for input/output asynchronous sequential machines with disturbance inputs. An unobservable and uncontrollable disturbance input can infiltrate into asynchronous machines and provoke unauthorized state transitions. We present the existence condition for a corrective controller that automatically counteracts the effects of disturbance inputs and restores desirable behavior to the controlled machine. Unlike input/state asynchronous machines, access to the machine's state is not available in the control procedure of input/output machines, so the control scheme requires state observation and fault detection modules. As a case study, the architecture of an asynchronous clock divider with the corrective controller is implemented and experimental verification on FPGA is provided for showing the applicability of the proposed controller.

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1. Introduction

Asynchronous sequential machines are event-driven. They respond immediately to the completion of a computation without waiting for a clock edge. With this feature, asynchronous machines offer substantial benefits in the design of digital control units or sequencers, particularly when many actions of the control unit are based on externally generated signals that are not guaranteed to be correlated with an available clock signal [3,7]. As an important building block of high-speed digital computers and control systems, asynchronous machines are still being widely used in various areas such as parallel computation [21], system-on-chip design [17], and nuclear engineering [29].

The objective of this paper is to propose a robust controller for asynchronous sequential machines suffering from adverse effects of disturbance inputs [2,20,23]. For asynchronous machines working in safety–critical applications, the attack of disturbance inputs that represent unmeasurable noise or unauthorized and adversarial agents turns out to be an inevitable feature [1,29,32]. In particular, we focus our concern on the *state fault*, where disturbance inputs breaking into the asynchronous machine cause unauthorized state transitions so that the behavior of the machine would be unpredictable thereafter if not recovered immediately.

Our approach is based on *corrective control* proposed by Murphy et al. [19] and Geng and Hammer [6], in which an asynchronous machine is regarded as a system to be controlled so that the stable state behavior of the machine is compensated or "corrected" by a feedback controller that is constructed as another asynchronous machine. Corrective control is worth researching since it is a novel scheme for changing the input/output specification of the machine without resort to re-design of the machine's inner logic. In the former studies, corrective control was developed mainly to match the behavior of the closed-loop system to a prescribed model while eliminating malfunctions lying in the machines, e.g., critical races [19], infinite cycles [30] and adversarial inputs [34,35].

* Corresponding author. Tel.: +82 53 580 5926; fax: +82 53 580 5165.
E-mail address: ksw@kmu.ac.kr (S.W. Kwak).

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The present research continues the investigation into the control of asynchronous sequential machines with disturbance inputs initiated in [34,35]. Compared to [34,35] and other approaches on digital systems design [8], this paper has the following contributions.

(1) First, the considered asynchronous machine is input/output type, whereas the previous studies [34,35] were developed on input/state asynchronous machines. Input/output type is a more general representation of asynchronous machines since a majority of systems have the output domain different from the state set. For instance, an encoder with sequential logic has inner states that are changed according to the encoding process, while the encoder output, determined by the encoding logic, is in general different from the state. Since access to the state is not available in input/output machines, the controller needs state observation and fault detection modules for catching any state fault caused by disturbance inputs. Note that Geng and Hammer [6] also tackled the problem of controlling input/output asynchronous machines by proposing detectability and the state observer. Their control objective, however, is model matching for nominal machines with no disturbance input, i.e., to design a corrective controller so that the closed-loop system exhibits desirable characteristics. To deal with disturbance inputs and state faults, a novel notion of state observation and detectability must be developed, the latter of which will be termed *fault detectability* in this paper.
(2) Secondly, the previous studies [34,35] as well as the other related researches on corrective control [19,6,30] were developed only in a theoretical framework and did not include experimental results. In contrast, this paper provides a hardware implementation of the proposed controller on FPGA. The experimental verification will validate that the theory of corrective control on asynchronous machines, though modeled in abstract finite state machines, can be implemented in a real asynchronous digital circuit.

In the field of systems with event driven dynamics with discrete state space, the research on fault diagnosis and recovery tasks has already gained particular attention. In [4], a novel reconfiguration scheme is proposed for fault-tolerant mesh topology with redundant nodes and links. Yan and Wang [33] addresses the problem of fault diagnosis agreement (FDA) for general networks. Rigatos [24] presents a fault diagnosis scheme based on fuzzy automata, while [25] uses fuzzy automata for addressing adaptive fault-tolerant routing algorithms in interconnection networks. The readers are also referred to [27,37,2,26] for issues related to fault diagnosis and tolerance in discrete event dynamic systems. But these former studies do not address certain issues that are critical to the operation of asynchronous sequential machines, like the distinction between stable and transient states and fundamental mode operation as will be discussed in our study.

Not only in discrete event systems but in continuous time systems, fault-tolerant control (FTC) has been a focus of increasing research investigation over the past few decades. Among notable recent results in continuous time systems, there are the discrete time FTC systems [15,16], FTC for Takagi–Sugeno fuzzy models [38,31], FTC with the dissipativity-based switching scheme [10], FTC with sliding mode control technique [36,14], and FTC in the form of adaptive output–feedback controllers [9,18].

Fault tolerance is also one of active research topics in the design and manufacture of VLSI circuits and network-on-chip (NoC). Das et al. [5] reports new space compression techniques for realizing fault tolerance in VLSI design. In [12], a self-contained adaptive system is proposed for detecting and bypassing permanent errors in network-on-chip interconnects. Both studies utilize redundancy lying in system resources for securing fault tolerance capability, which is somewhat similar to the notion of corrective control. However, for the same reason as the preceding literature, they are not applicable to asynchronous sequential machines.

This paper is organized as follows. Section 2 reviews and expands the basic notation and framework of our discussion. In particular, a model of input/output asynchronous machines is presented where a disturbance input penetrates into the machine and triggers undesirable state transitions. In Section 3, the structure of the proposed control scheme is described. A corrective controller is connected before the considered machine, and a state observer, placed on the output feedback line, observes the present state of the machine and detects state faults. The controller takes state recovery action whenever a fault is detected, i.e., it drives the machine to the original state very quickly (ideally in zero time), thus making the closed-loop system fault-tolerant against state faults. In Section 4, the structure of the observer used in the control scheme is presented. Section 5 presents necessary and sufficient conditions for the existence of an appropriate controller. Whenever controllers exist, algorithms for their design are outlined. In Section 6, the architecture of an asynchronous clock divider with the corrective controller is introduced as a case study, and experimental verification on FPGA is provided for showing the applicability of the proposed controller. Finally, some concluding remarks are addressed in Section 7.

2. Input/output asynchronous machines

An asynchronous sequential machine is represented by the following finite state machine:

$$\Sigma = (A, Y, X, x_0, f, h), \tag{1}$$

where A is the input set, Y is the output set, X is a set of q states, and x_0 is the initial state. Since we deal with the situation where a disturbance input penetrates into asynchronous machines through the input channel, we divide A into two mutually exclusive subsets—the normal input set A_n and the disturbance input set A_d, i.e., $A = A_n \cup A_d$. If $A_d = \emptyset$, Σ is reduced to a

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