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Design and analysis of a transformerless STATCOM based on hybrid cascaded multilevel converter

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ABSTRACT

This paper presents a new concept of Static Synchronous COMpensator (STATCOM) based on a Hybrid Cascaded Multilevel Converter (HCMC). The HCMC consists of a two- level voltage converter and a wave-shaping circuit formed by cascaded H-bridge Sub-Modules (SM). Firstly, the operation principle and overall control strategy of HCMC are presented. After that, some key parameters including size of capacitors, numbers of sub-modules are in-depth analyzed. And then, a thorough comparison between the proposed HCMC-based STATCOM and conventional cascaded H-bridge based STATCOM is made, which turns out that the proposed HCMC-based STATCOM requires less number, size and stored energy of capacitors and has less power loss. Finally, a 35 kV/ ± 50 Mvar HCMC-based STATCOM simulation model is constructed in PSCAD/EMTDC software platform. The simulation results validate the feasibility of the proposed HCMC-based STATCOM and the correctness of the analysis.

1. Introduction

Static synchronous compensator (STATCOM) using voltage source converter is a flexible ac transmission system (FACTS) device for generating or absorbing reactive power. With reactive power compensation in power system, voltage regulation and maximum power transmission can be achieved [1–13].

Different kinds of STATCOMs have been tested and installed in many electrical networks during the past few decades [1–5]. Many kinds of multilevel converters, such as (1) diode-clamped converter, (2) flying-capacitor converter, (3) cascaded H-bridge converter [7–13], modular multilevel converter (MMC) [14–17], alternate arm converter (AAC) [18–20], can be used as STATCOM. The multilevel structure provides redundancy and scalability. However, it requires a fairly large number of H-bridge sub-modules to reduce the harmonics and each sub-module requires a large DC capacitor.

This paper proposes a novel STATCOM based on hybrid cascaded multilevel converter (HCMC), which is a newly introduced voltage-source converter [21]. As shown in Fig. 1, it has two key parts, i.e., the two-level converter and the wave-shaping circuit (WSC) containing cascaded H-bridge sub-modules. The two-level converter is arranged to operate at fundamental frequency with square-wave modulation, which reduces switching loss and simplifies dynamic voltage sharing along the series string of IGBTs [20]. The overall rating of the STATCOM is shared between the two-level converter and the wave-shaping circuit, with the result that fewer sub-modules are needed in the wave-shaping circuit in comparison with the cascaded H-bridge STATCOM. This is particularly beneficial in reducing the required number and rating of DC capacitors, which dominate the size and weight of the converters [21]. To achieve stable operation, the coordination and synchronization between the two-level converter and the wave-shaping circuit are required.

This paper focuses on the principle, control scheme of the proposed STATCOM and the sizing of the DC capacitors. The outline of this paper is organized as follows: The operation principle of the proposed STATCOM will be discussed in Section 2. Section 3 proposes a control scheme for this proposed STATCOM. Section 4 establishes the DC voltage ripple equations and the criterion for sizing the DC capacitors of the two-level converter and the wave-shaping circuit, respectively. Section 5 gives the comparison of the number of IGBTs and the number, size and stored energy of the DC capacitors between the proposed STATCOM and the cascaded H-bridge STATCOM. The feasibility of the HCMC-based STATCOM is verified by simulation results in Section 6. Section 7 concludes the paper.

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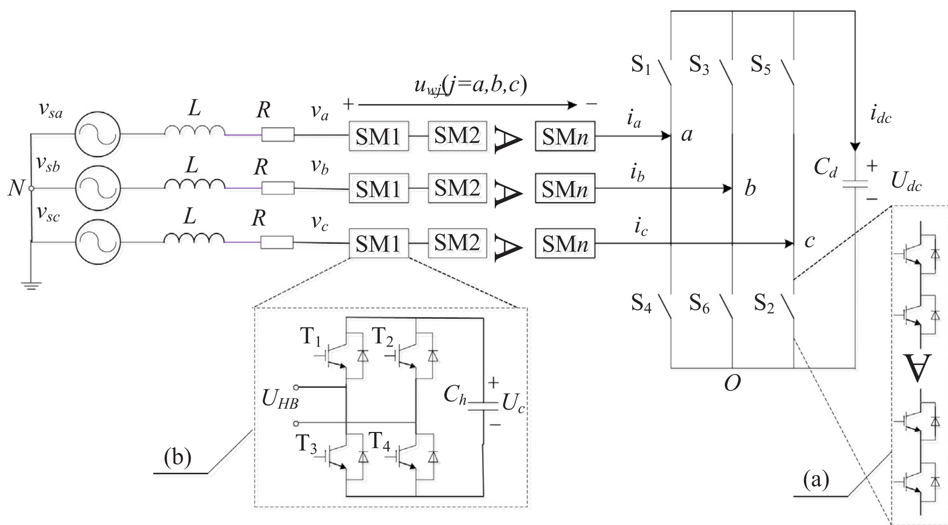

Fig. 1. Main circuit configuration of proposed STATCOM. (a) IGBTs connected in series in the two-level converter. (b) H-bridge sub-module structure.

2. Proposed statcom and its operation principle

2.1. Main circuit configuration

The three-phase main circuit configuration of the proposed STATCOM is illustrated in Fig. 1. The WSC composed of the cascaded H-bridge sub-modules is placed on the AC side. Each arm of the two-level converter consists of series-connected IGBTs shown in Fig. 1(a). Fig. 1(b) illustrates the H-bridge structure, whose output voltage UHB has three states: (1) $+Uc$; (2) $-Uc$; and (3) 0. Here, Uc is the rated voltage of the capacitor. This means each sub-module has three states in normal operation: (1) positively inserted ($UHB = Uc$); (2) negatively inserted ($UHB = -Uc$); and (3) bypassed ($UHB = 0$).

2.2. Operation principle

The two-level converter is arranged to operate at fundamental frequency (50 Hz) by using square-wave modulation, producing a square wave at its AC terminal. The wave-shaping circuit constructs multilevel output voltage and compensates the difference between the output of the two-level converter and the desired (sinusoidal) voltage. It operates as a series active power filter to attenuate the voltage harmonics produced by the two-level converter. Thus, the output voltage of HCMC is almost purely sinusoidal, making a significant improvement compared to the traditional two-level converter.

Fig. 2 illustrates the basic single-phase equivalent circuit and reference voltage waveforms of the STATCOM, where v_{sa} is the grid voltage of phase a, u_{aN} is the output voltage of the two-level converter in phase a, and L and R are the total equivalent AC inductance and resistance. From Fig. 2(a), the basic characteristics of the STATCOM can be described as follows:

$$v_{sa}(t) = U_m \sin \omega t \tag{1}$$

$$i_a(t) = I_m \sin(\omega t + \pi/2) = I_m \cos \omega t \tag{2}$$

$$v_a(t) = u_{wa}(t) + u_{aN}(t) \tag{3}$$

$$u_{aN}(t) = M_a U_{dc} \tag{4}$$

$$u_{wa}(t) = \sum_{j=1}^{N} G_j U_{cj} \tag{5}$$

where U_m denotes the phase voltage amplitude, v_a is the output voltage of the STATCOM of phase a, I_m denotes the current amplitude, M_a denotes the switching factor which is determined by the states of the switches in the two-level converter, U_{dc} is the voltage of the DC capacitor of the two-level converter, N is the number of H-bridge sub-modules per phase, U_{cj} ($j = 1,2,\ldots,N$) is the capacitor voltage of the jth H-bridge sub-module, and G_j is the switching function corresponding to the three operation states of the jth H-bridge sub-module ,i.e., positively inserted ($G_j = 1$), negatively inserted ($G_j = -1$), and bypassed ($G_j = 0$).

2.3. Analysis of U_{dc} and N

When the number of the H-bridge sub-modules per phase N and the rated voltage of the H-bridge capacitors U_c are specified, the output voltage range of the cascaded H-bridge cells is determined as follow:

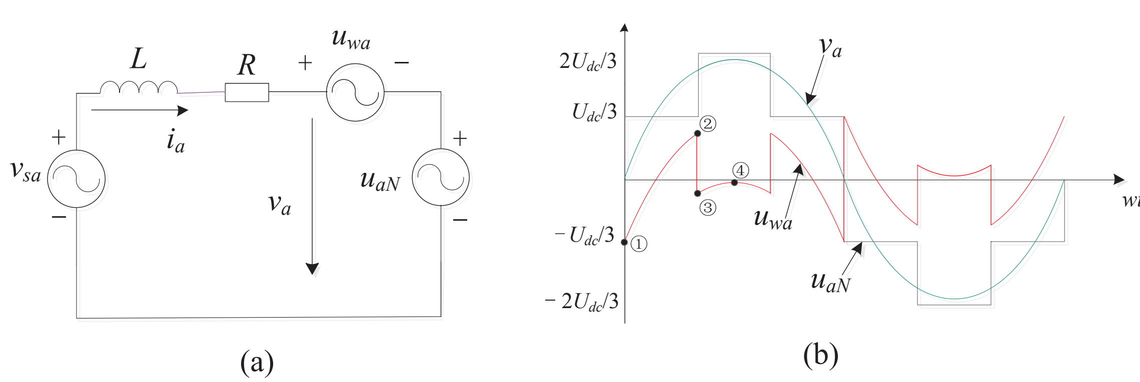

Fig. 2. Single phase equivalent circuit and reference voltage waveforms. (a) Single phase equivalent circuit of the system. (b) Reference voltage waveforms.