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Design and implementation of flexible Numerical Overcurrent Relay on FPGA

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ABSTRACT

This paper presents the contemporary design and implementation of an intelligent revelation in the field of the over-current relay to meet the challenges of the modern grid. The unique three-neuron single layered architecture of Artificial Neural Network (ANN) provides flexibility by exploiting its universal function approximation capabilities. The Unique Selling Proposition (USP) of the present development is the simple design of ANN, suitable for low-end, low-cost Field Programmable Gate Array (FPGA) implementation. The nano-scaled internal processing time for three-phase design, with the provision of remotely controlled adaptive relay settings, would definitely an innovative solution for grid connection of renewable energy sources. The proposed design of the universal over-current relay, confirmed by the real-time testing, is a true fusion of electrical power, communication and information technology to meet the global trend of the electrical power industries.

1. Introduction

Evolution of protective relays began with sluggish and expensive electromechanical relays, then relatively cheaper and efficient solid state relays and finally to modern and advanced digital/numeric relays. Conventional electromagnetic relays have several drawbacks such as high burden on instrument transformers, high operating time, contact problems etc. Static relays increasingly and successfully used for past few years suffer from a number of demerits like less flexibility, duplication of specific effort, non-adaptability to changing system condition, complexity and cost [1–3]. But the concept of digital protection employing microprocessor/microcontroller can eliminate some of the limitations of electromagnetic and solid state relays easily [1–3]. The main features which have encouraged and attracted power engineers to design and develop the digital protection schemes are their economy, compactness, reliability, flexibility, expandability, ease of communication, ease of maintenance and improved performance over electromagnetic, static relays. But microprocessor and microcontroller based systems also have some pitfalls such as limitations of data size, floating-point operation, physical overheating, not bit addressable, sequential operation etc. [4–10].

Modern Power System has tremendously grown both in size and complexity. The conventional relays including the over-current relay (OCR) operate with the fixed manual setting. It is difficult to ensure proper protection when operating condition of the radial distributing systems are changing in the context of a smart grid, due to insertion of distribution generations (DGs). Hence, the modern power system demands an intelligent and adaptive protection scheme where the relay can automatically configure its characteristics or settings when the network status changes [11–16]. Another parallel evolution in the area of the embedded system is programmable hardware for implementing the digital logic. Field Programmable Gate Arrays (FPGAs) falls under this category. FPGA is a reconfigurable integrated circuit that offers flexible and robust design capabilities. Implementation of parallel working modules on a single chip is possible [17–18]. This is why in recent years the concept of FPGA based relays are considered of great importance [19–21]. These relays are reconfigurable, robust in nature. Relays can be operated with higher speed, accuracy, and efficiency. Infact parallel processing is the key feature of FPGA while Microcontroller/microprocessor and DSP are sequential devices which make FPGA a desirable embedded platform for hardware implementation purpose. All these digital relays having good compatibility, reliability, flexibility and continued reduction in digital circuitry makes it favorable to open new ventures in this field.

Artificial Neural Networks (ANN) is a parallel processing soft-computing paradigm which provides a simple and efficient method to implement various non-linear input-output mapping. It is also known as “Universal Function Approximator” [22]. However, lack of simple hardware design that is capable of adopting any changes in the operating environment of the system limits the applicability of ANN in the

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industrial environment [23–26]. The overcurrent relays are most commonly used as a protective device for radial distribution systems, large motors, alternator, transformers, expensive cables etc. The conventional digital over-current relays fail to provide intelligent adaptive protection [1–4,6,16]. Various types of digital relaying techniques have been reported in the last decade [1–4,6,16–21]. But these designs lack two major issues (i) adaptability and (ii) smart logic. Implementation of digital OCRs using microprocessor or micro-controller has been reported in [1–3]. FPGA based system on programmable chip design for implementation of OCRs has been addressed by the previous researchers [17–21]. They have used either direct implementation of relaying characteristics or lookup tables to store them. These crude methods are neither hardware friendly nor adaptive in nature and moreover require huge resources. Keeping the above viewpoints in mind, the present development is an attempt and the first reporting of Artificial Neural Networks Based Overcurrent Relay implemented on FPGA that meets the demands of the modern power systems.

2. Design of ANN based flexible OCRs

In present design, the well-known IEC62055 standard [27] for the Overcurrent relay characteristics (viz. Inverse definite Minimum time (IDMT), Very Inverse (VI), and Extremely Inverse (EI)) have been considered. These nonlinear characteristics are furnished in Eqs. (1)–(3) respectively.

$$t(I) = \frac{0.14}{M^{0.02}-1} \times TSM \tag{1}$$

$$t(I) = \frac{13.5}{M-1} \times TSM \tag{2}$$

$$t(I) = \frac{80}{M^{2}-1} \times TSM \tag{3}$$

where $t(I)$ = Operating Time in sec.

M = Plug Setting Multiplier (PSM) = Actuating Current/Pick up current

TSM = Time Setting Multiplier

While targeting the FPGA as prototyping hardware, it is difficult to implement non-linear IDMT characteristic like Eq. (1) directly, due to its exponential terms in the order of 0.02. It is important to mention that, the previous researchers have avoided this IMDT characteristic in their work [20]. Under this constraint, ANN may provide a smart solution by exploiting its universal function approximation capabilities [22]. It is well known that a simple ANN model, as shown in Fig. 1, with suitable weights and bias, can map any kind of complex non-linear characteristics [28]. This feature of ANN has been utilized here to design the universal over-current relay.

ANN is a multiplication rich computational technique. On the other hand, low-end FPGA chips have limited numbers of “multipliers” [22,25,26,28]. Hence the selection of large ANN architecture for implementation of relay characteristics would put a ceiling on its economical implementation in low cost, low-end FPGA. Moreover, ANN with more than one hidden layer may cause a considerable amount of propagation errors. Hence the present design has been focused on a feed-forward ANN architecture with a single hidden layer. Logsigmoidal activation functions were used in the hidden layer neurons to justify the nonlinear input out mapping of the relay characteristics.

The optimal architecture along with its free weights and bias among neurons have been selected after careful off-line training of the ANN

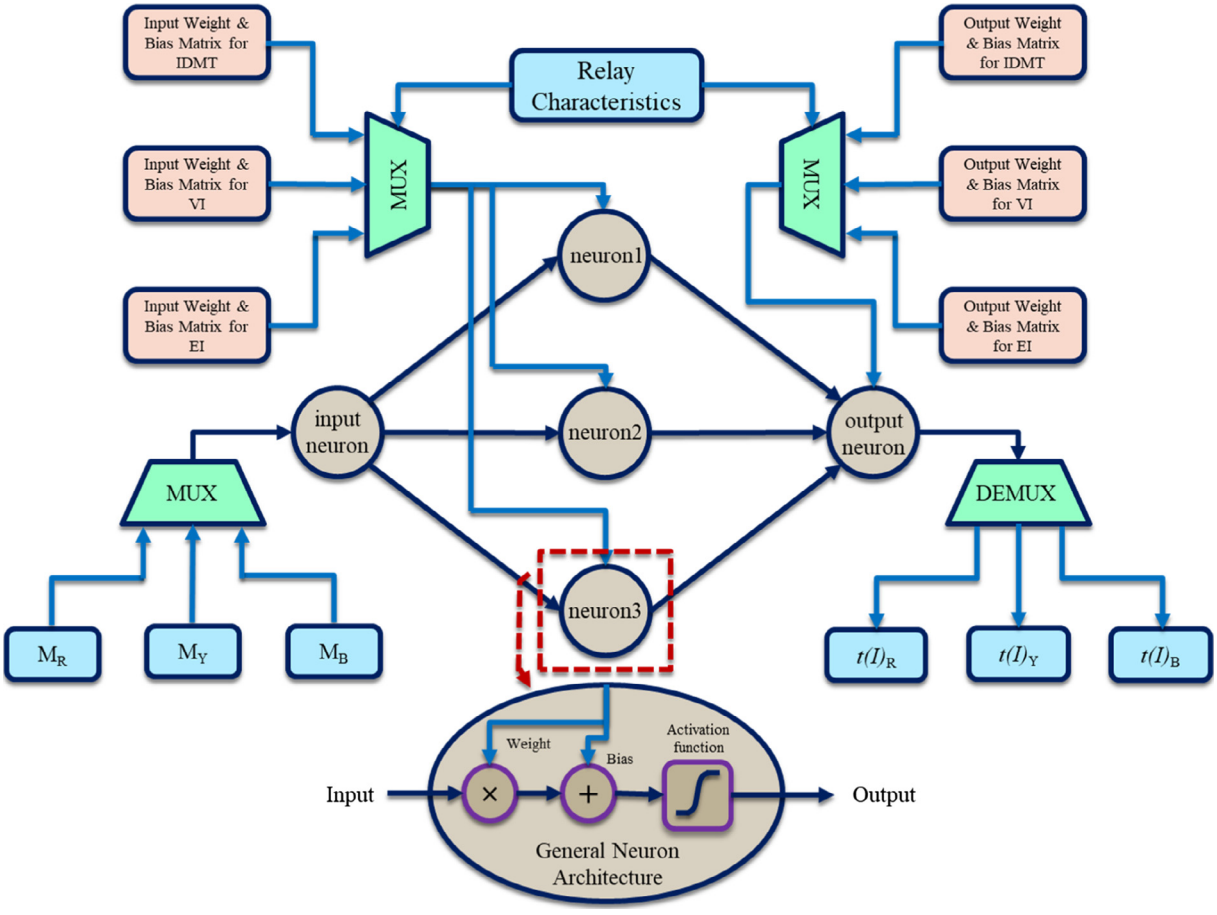

Fig. 1. ANN model of a single hidden layer with three neurons developed in MATLAB.