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## An improved finite control-set model predictive control for nested neutral point-clamped converters under both balanced and unbalanced grid conditions



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#### ARTICLE INFO

#### ABSTRACT

Keywords: Finite control-set model predictive control Nested neutral point-clamped converters Flexible power regulation Dynamic references Unbalanced grid conditions Finite control-set model predictive control (FCS-MPC) is an alternative strategy, in particular, for multi-level converters. However, the computational burden is rapidly increased with the number of voltage vectors to be predicted and objectives to be controlled. This will hinder the development of the FCS-MPC strategy. In this paper, an improved FCS-MPC is proposed for nested neutral point-clamped converters (NNPCs) under both balanced and unbalanced grid conditions. Specifically, to reduce the computational burden, an optimized voltage vector selection process based on deadbeat technique is embedded into the proposed design. Meanwhile, a simplified cascade-free control strategy is presented to directly govern the DC-link voltage and reactive power in NNPCs while the flying capacitor voltages are maintained balanced. Moreover, the inclusion of a power compensation approach is presented for the FCS-MPC method in an attempt to obtain desired grid-side currents under nonideal grid-side voltage conditions. The novelty of this work lies not only in a compatible reference design that directly allows to formulate the optimal control problem using a simplified cascade-free control strategy robust the proposed FCS-MPC and the power compensation technique for suppressing the distorted grid-side currents under unbalanced grid conditions. The performance of the proposed strategy for NNPCs is evaluated by simulation studies in various operating conditions.

#### 1. Introduction

The nested neutral point-clamped converters (NNPCs) have gained tremendous attention in medium-voltage high-power (MV-HP) applications, such as distributed generation systems, smart grid technologies, and motor drives. The authors in [1] firstly propose the NNPCs topology. This topology is a combination of a flying capacitor topology with a neutral point-clamped converter topology, which provides four levels in output voltage without the need for connecting the power semiconductor in series. Compared to the traditional two/three-level three-phase grid-converters, NNPCs provide several merits including grid-side currents with low-harmonic distortion, low voltage stress on switches, low switching frequency, and less switching losses. These remarkable features attracted the different research institutions, especially in MV-HP power electronics [2–4].

In recent years, various control techniques and modulation strategies have been proposed for NNPCs [5–7]. In [5], a novel sinusoidal pulse width modulation (SPWM) technique for NNPCs is applied to each leg separately to generate output waveforms. Although the study [5] yields excellent performance, the influence of common-mode voltages is not investigated. An improved method using space vector modulation (SVM) is proposed to mitigate the common-mode voltages in dynamical systems in [6]. To synthesize given reference vectors, three switching states with respect to minimal absolute common-mode voltages are used in the proposed strategy. Thus, the common-mode voltages can be suppressed effectively. In [7], simple logic tables are employed to control the voltage-balancing of flying capacitor. This method is suitable for and can be easily integrated with different pulse width modulation (PWM) schemes such as SPWM and SVM. Although, satisfactory control performance can be obtained due to its strong adaptability and reliability, the system dynamic performance will be limited by the fixed PI parameters during disturbances. Besides, the selection of control parameters needs careful deliberation since they have a profound influence on the stability of the overall control system.

In contrast to linear control, finite control-set model predictive control (FCS-MPC) approach, which is based on a nonlinear control

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method, is proposed in [8]. The main characteristics of this method relies on discrete nature of power converters to predict the future behavior of the controlled variables, without requiring any pulse-width modulators, switching table, or PI controller [9-11]. In comparison with traditional control methods, the FCS-MPC has many advantages, such as excellent dynamic performance, easiness to include different control objectives, and the ability to address multiple constraints [12-14]. Although satisfactory results can be obtained with such a strategy, it has a higher computational burden, especially under high voltage-levels [15]. This will limit the application of the FCS-MPC scheme in practice. Besides, the control performance of the FCS-MPC method for NNPCs will be affected under unbalanced grid voltage conditions. Motivated by this limitation, many researchers have attempted to mitigate the influence of unbalance grid voltage on FCS-MPC [16-18,24,25]. To the best of the authors knowledge, although there are a great number of works regarding the FCS-MPC strategy, the investigation on the power compensation method for NNPCs using a simplified cascade-free FCS-MPC under unbalanced grid conditions has not been reported.

In this paper, an improved FCS-MPC for NNPCs under both balanced and unbalanced grid voltage conditions is proposed. It takes the simplified computational strategy and dynamic references design into account simultaneously. To reduce the computational burden, a sector distribution method based on SVM is embedded into the proposed design. Specifically, a combination of SVM with deadbeat-predictive direct power control (DB-PDPC) solution is employed to reduce the calculation efforts. Meanwhile, in order to enhance the dynamic performance, a dynamic reference design with a simplified cascade-free FCS-MPC strategy is deployed. Thus, the tracking of the DC-link voltage favors excellent transient characteristics with reduced complexity while keeping the flying capacitor voltages balancing. Moreover, the inclusion of a power compensation scheme is presented for the FCS-MPC method in an attempt to obtain desired grid-side currents under nonideal grid-side voltage conditions. In this sense, the negative-sequence grid-side current component is not needed to be extracted. In our work, the comparison of different published works in [24,25] with nonideal grid-side voltage conditions is investigated. Compared with the previously reported FCS-MPC methods dealing with the same challenge, the proposed method can provide an excellent steady-state performance and fast dynamic response while remaining computationally feasible.

The contribution of the proposed method is summarized as follows: i) Compared with the conventional FCS-MPC method in [8] and the proposed method in [20], a simplified cascade-free control strategy is proposed to directly govern the DC-link voltage and reactive power in NNPCs while the flying capacitor voltages are maintained balanced. The proposed strategy avoids the using of external PI controller (outer loop) without any integrator windup phenomenon. Hence, the flexible active power control becomes feasible and has excellent dynamic characteristics. Meanwhile, it does not need the dq synchronous reference frame, switching table, PI controller, or PWM modulators. The proposed controller calculates the required active power reference based on the output power and the energy stored in the DC-link capacitor. The active power and current constraints are included inside the cost function. When the constraints are fully respected, no overlimit charging and discharging current occurs. In this work, the proposed scheme is suitable when considering the lifespan of the DC-link capacitor. ii) Compared with the conventional FCS-MPC methods in [8,9,11,13,14] and the simplified FCS-MPC method in [21], a power compensation scheme based on a simplified FCS-MPC algorithm for NNPCs is presented to suppress the distorted grid-side currents in the  $\alpha\beta$ stationary reference frame under unbalanced grid conditions. Meanwhile, the design of predictive controller takes the advantage of enhancing the control flexibility of the NNPCs, and restricting the total harmonic distortion (THD) in grid-side currents without increasing the controller complexity. Thus, distorted grid-side currents can be suppressed effectively while remaining computationally feasible.

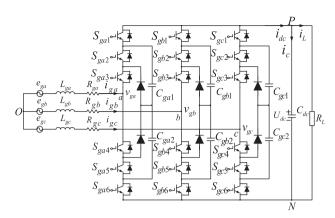


Fig. 1. The common topology of the NNPCs.

The rest of this paper is organized as follows. The FCS-MPC method for NNPCs is briefly introduced in Section 2. The dynamic references design with the simplified cascade-free FCS-MPC scheme for NNPCs is presented in Section 3. In Section 4, the power quality improvement under unbalanced grid voltage conditions is described. To validate the performance of the proposed method, compared simulations for two different control schemes are investigated in Section 5. Section 6 concludes the work in this paper.

#### 2. FCS-MPC method of NNPCs

The circuit topology of the NNPCs is shown in Fig. 1. Each phase of the NNPCs includes 6 switches, 2 clamping diodes, and 2 flying capacitors. The voltage of each flying capacitor should be kept at one-third of DC-link voltage ( $U_{dc}/3$ ) to ensure that all the power switches share the same voltage stress ( $U_{dc}/3$ ).

In a natural reference frame, the grid-side and rectified-side models for the system in Fig. 1, to predict the grid current and the rectified voltage, are obtained from

$$\begin{cases} L_{ga} \frac{di_{ga}}{dt} = e_{ga} - v_{ga} - R_{ga} i_{ga}, \\ L_{gb} \frac{di_{gb}}{dt} = e_{gb} - v_{gb} - R_{gb} i_{gb}, \\ L_{gc} \frac{di_{gc}}{dt} = e_{gc} - v_{gc} - R_{gc} i_{gc}, \\ C_{dc} \frac{dU_{dc}}{dt} = i_{dc} - \frac{U_{dc}}{R_L}, \end{cases}$$

$$(1)$$

where

and where

$$\nu_{NO} = -\frac{1}{3}(\nu_{gaN} + \nu_{gbN} + \nu_{gcN}), \tag{3}$$

and  $e_{ga}$ ,  $e_{gb}$ , and  $e_{gc}$  represent input voltage vector, respectively.  $i_{ga}$ ,  $i_{gb}$ , and  $i_{gc}$  represent input current vector, respectively.  $L_g$  represents input coupling inductance value,  $R_g$  represents input resistance value,  $U_{dc}$  is DC-link/rectified voltage,  $C_{dc}$  is DC-link capacitor value,  $i_{dc}$  is rectifier dc current, and  $R_L$  is load resistance value.  $v_{ga}$ ,  $v_{ga}$ , and  $v_{ga}$  represent the voltages generated by the NNPCs with respect to the grid neutral *O*.  $v_{gaN}$ ,  $v_{gbN}$ , and  $v_{gcN}$  represent the voltages between any phase  $x = \{a, b, c\}$  of the NNPCs and the negative point of the DC-link *N*,  $v_{NO}$ is the voltage between the negative point of the DC-link *N* and the grid neutral *O*. Considering a constant DC-link voltage and balanced flying capacitor voltages, the voltages generated by the NNPCs are obtained from Download English Version:

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