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Steady-state performance of state-of-the-art modular multilevel and alternate arm converters with DC fault-blocking capability

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ABSTRACT

This paper presents a comparison of the steady-state behaviour of four state-of-the-art HVDC converters with DC fault-blocking capability, based on the modular multilevel and alternate arm converter topologies. AC and DC power quality, and semiconductor losses are compared, whilst considering different operating conditions and design parameters, such as the number of cells and component sizing. Such comparative studies have been performed using high-fidelity converter models which include detailed representation of the control systems, and of the converter thermal circuit. The main findings of this comprehensive comparison reveal that, the mixed cell modular converter offers the best design trade-off in terms of power losses and quality, and control range. Moreover, it has been established that the modular converter with a reduced number of cells per arm and with each cell rated at high voltage (i.e. 10–20 kV), tends to exhibit higher switching losses and relatively poor power quality at the DC side.

1. Introduction

The rapid growth of renewable energy production, particularly from remote offshore wind farms, requires efficient transmission system technology, which can transmit power and support both offshore and onshore grids. Existing multilevel voltage source converter based High Voltage Direct Current (HVDC) transmission systems, have received universal acceptance from the power industry. This is due to the fact that they satisfy the aforementioned requirements, offer high efficiency and high power quality at both AC and DC sides, and provide internal fault management which is critical for facilitation of continuous operation during cell failure [1–3].

Reverse-blocking converters (or simply converters with DC fault blocking) are increasingly important as they provide a means to ride-through solid DC short-circuit faults, with only short periods of power interruption between the connected AC grids. This is achieved without significant impact on voltage stability as the reverse-blocking converters can prevent or control the AC-side contribution to the DC fault current. Hence, reactive power within connected AC grids, will be no longer flowing uncontrollably. In multi-terminal HVDC networks which utilise reverse-blocking converters, DC-link voltage remains at zero after fault clearance, as long as the converter terminals remain blocked. This clearly provides the opportunity for complete replacement of expensive DC circuit breakers with lower-cost DC disconnectors [4]. Typical modern multilevel HVDC converters, have complex power circuit structures with complex internal dynamics (inter-cell, inter-arm and inter-phase dynamics), that require a number of well-designed dedicated controllers to ensure converter stability over the entire operation range [5–8]. Analytical performance evaluation of such converters is time-consuming and could be ineffective. For example, it is cumbersome to account for the effect of complex Capacitor Balancing Algorithms (CBAs) in average models. This is due to the fact that CBAs affect the average switching frequency per switching device (switching loss), arm energy balance and inter-arm dynamics, and hence, average models are unable to reproduce such effects [9,10].

Several attempts have been made to estimate semiconductor conduction and switching losses in modular multilevel converters [11–14], however, numerous calculation of losses found in the open literature, differ significantly. For example, estimation of semiconductor losses for a half-bridge modular converter varies from 0.3% to 1% [11,12]. This is because some of these studies do not account correctly for important considerations such as the CBA and modulation, redundancy, and temperature effects. In contrast, detailed estimation of semiconductor losses for several modular and hybrid converters, including mixed-cell MMC and AAC, have been presented in [13] including the impact of different modulation methods. However, this study neglects thermal

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effects and the possibility of incorporating redundant cells. As in previous studies, the loss estimations presented in [14] are extremely low, and opposite to widely accepted figures for conversion losses in modular and hybrid type converters [11,13].

At present, there are two competing approaches to the realisation of modular multilevel converters. The first approach utilises a large number of cells per arm, where the blocking capability of each cell is small and is defined by the rating of a single switching device (i.e. 2–3 kV). The second approach adopts a reduced number of cells per arm, with each cell rated for high DC operating voltage, ranging between 16–20 kV. Thus, the latter approach requires the adoption of series-connected semiconductor devices. To date, no detailed studies available in the open literature have investigated the potential impact of a reduced number of cells on power quality, both on AC and DC sides but also on semiconductor losses in the MMC. Similar research gaps have been identified on the analysis of the AAC, particularly with regard to power quality on the DC side.

This paper presents a novel research approach which utilises detailed converter models (developed in EMTP-RV [9,15]) and a well-designed set of test scenarios. The ultimate goal is to compare the performance of different converters, with emphasis given to Alternate Arm Converter (AAC) [16] and Modular Multilevel Converter (MMC) [17] and its derivatives, namely the Mixed-Cell MMC (MC-MMC) [18]. The main performance indicators used in the comparison are (i) capacitor voltage ripple, (ii) cell capacitance or energy storage requirement per converter, and (iii) semiconductor losses. Both MMC and AAC topologies include full-bridge cells which can reverse the cell voltage polarity and therefore block DC current [19,20]. Both Full-Bridge MMC (FB-MMC) and Half-Bridge MMC (HB-MMC) are investigated [5], even though the HB-MMC does not have blocking capability. Also this paper presents a concise description of the operating principles and modelling of each converter topology, including the formulae which govern operation, and accurately reflects the internal and external dynamics, thermal behaviour and semiconductor losses. The main results obtained from these models are thoroughly discussed and the main factors that affect the power quality on the AC and DC sides, losses and potential design trade-offs are identified.

2. Converter modelling

This section briefly reviews the theoretical background which underpins the operating principles, control, and modelling of the MMC and AAC. A generic method for estimating semiconductor losses, which takes into account the effect of temperature on conduction and switching losses, is also presented.

Fig. 1 shows one phase leg, each for generic MMC and AAC circuits with N_{cell} number of cells per arm with subscript j defines the phase index (i.e. $j = a,b,c$) and k defines the upper and lower position of the arm (i.e. $k = u$ for the upper arm and $k = l$ for the lower arm).

2.1. Brief review of MMC

From Fig. 1 the cell capacitor current of each individual cell can be described in terms of arm current $i_{j,k}$ and the switching function $s_{cell-n_{j,k}}$ $\{-1, 0, 1\}$ as stated in (1):

$$i_{cell-n_{j,k}} = (1-s_{cell-n_{j,k}})\cdot i_{j,k} \tag{1}$$

Each arm voltage $v_{arm_{j,k}}$ (3) is formed by the summation of individual cell voltages $v_{cell-n_{j,k}}$ as described in (2):

$$v_{cell-n_{j,k}}(t) = \frac{1}{C_{cell}}\cdot \int_{t-\Delta t}^{t} (i_{cell-n_{j,k}}(t))dt \tag{2}$$

where Δt is the time step of the discrete integration.

$$v_{arm_{j,k}} = \sum_{i=1}^{N_{cell}} [(1-s_{cell-n_{j,k}})\cdot v_{cell-n_{j,k}}] \tag{3}$$

The voltage across the DC link can be expressed in terms of the instantaneous upper and lower arm voltages ($v_{j,u}$,$v_{j,l}$) of the same phase leg:

$$V_{DC} = v_{j,u} + v_{j,l} \tag{4}$$

Considering Fig. 1(a), the following voltage equations can be defined:

$$\frac{V_{DC}}{2} = v_{j,u} + \frac{L_{arm}}{2}\cdot\frac{di_{j,u}}{dt} - L_{AC}\cdot\frac{di_{j,AC}}{dt} + e_j \tag{5}$$

$$\frac{V_{DC}}{2} = v_{j,l} + \frac{L_{arm}}{2}\cdot\frac{di_{j,l}}{dt} + L_{AC}\cdot\frac{di_{j,AC}}{dt} - e_j \tag{6}$$

where L_{arm} and L_{AC} are the arm and AC-side inductances respectively (as shown in Fig. 1a) and e_j is the AC-side grid phase voltage. The upper and lower arm currents in each phase can be expressed by (7) and (8) respectively [21]:

$$i_{j,u} = \frac{i_{j,AC}}{2} + i_{j,diff} \tag{7}$$

$$i_{j,l} = -\frac{i_{j,AC}}{2} + i_{j,diff} \tag{8}$$

where $i_{j,AC}$ and $i_{j,diff}$ are the AC output phase and differential currents respectively. Current $i_{j,diff}$ flows through the upper and lower arms (however does not contribute to the AC output current) and can be defined by (9):

$$i_{j,diff} = \frac{i_{j,u} + i_{j,l}}{2} = i_{j,DC} + i_{j,cc} \tag{9}$$

$$i_{DC} = i_{a,DC} + i_{b,DC} + i_{c,DC} \tag{10}$$

where $i_{j,DC}$ and $i_{j,cc}$ are the DC and circulating currents respectively and the latter occurs due to the unbalanced voltages between the upper and lower arms in each phase.

$$v_{j,diff} = \frac{V_{DC}}{2} - v_{j,u} = -\frac{V_{DC}}{2} + v_{j,l} = \frac{v_{j,l} - v_{j,u}}{2} \tag{11}$$

where $v_{j,diff}$ is the differential voltage between the upper and lower arms and can be considered as the electromotive force (EMF) generated in each phase.

2.2. Brief review of AAC

As illustrated in Fig. 1(b), each AAC arm consists of series-connected FB cells and a director switch (DS). Cell capacitor current and voltage can be described similarly to (1) and (2), and therefore voltage $v_{stack_{j,k}}$ is considered to be identical to arm voltage as described by (3). The operation principle of an AAC is a combination of an MMC and a two-level converter, and can be described by the following three distinctive stages [19]:

- Stage I: Single arm conduction
- Stage II: Overlap
- Stage III: Off-state

During Stage I, the arm voltage is equal to $v_{stack_{j,k}}$ and the arm current is equal to $i_{j,AC}$. In Stage II, the AAC operates as an MMC where both the upper and lower arms conduct simultaneously for a very short period of time, in order to re-balance the voltage across the upper and lower stacks. In Stage III, the DS in the outgoing arm is turned off to stop the current flow, and enable the outgoing arm to block the full DC voltage. The time frames in (12) summarize the operation of the AAC during Stages I, II and III.